

Project Name :GM7MxxP

Platform : CFL-HR+N18E-GXR

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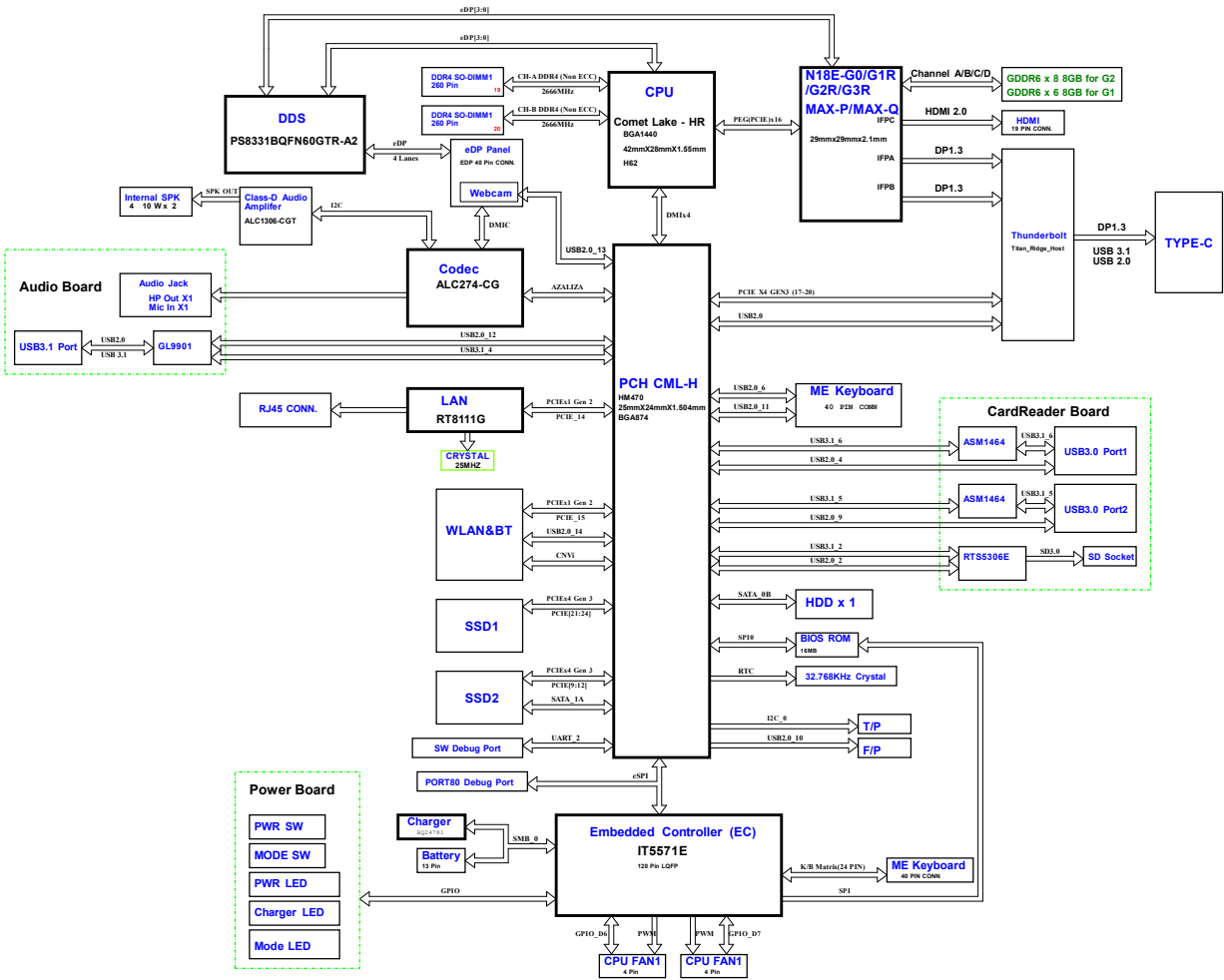
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

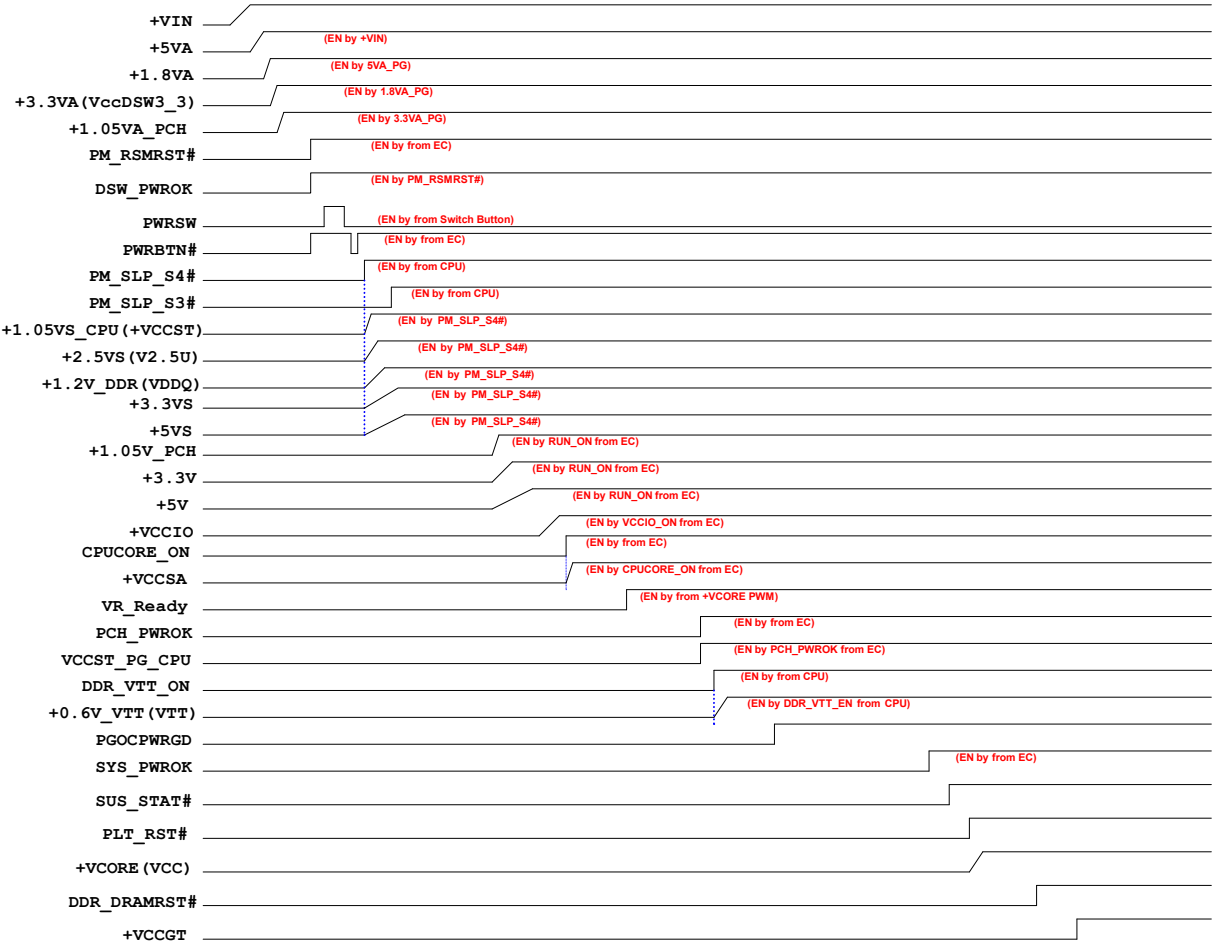
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

SYSTEM BLOCK DIAGRAM

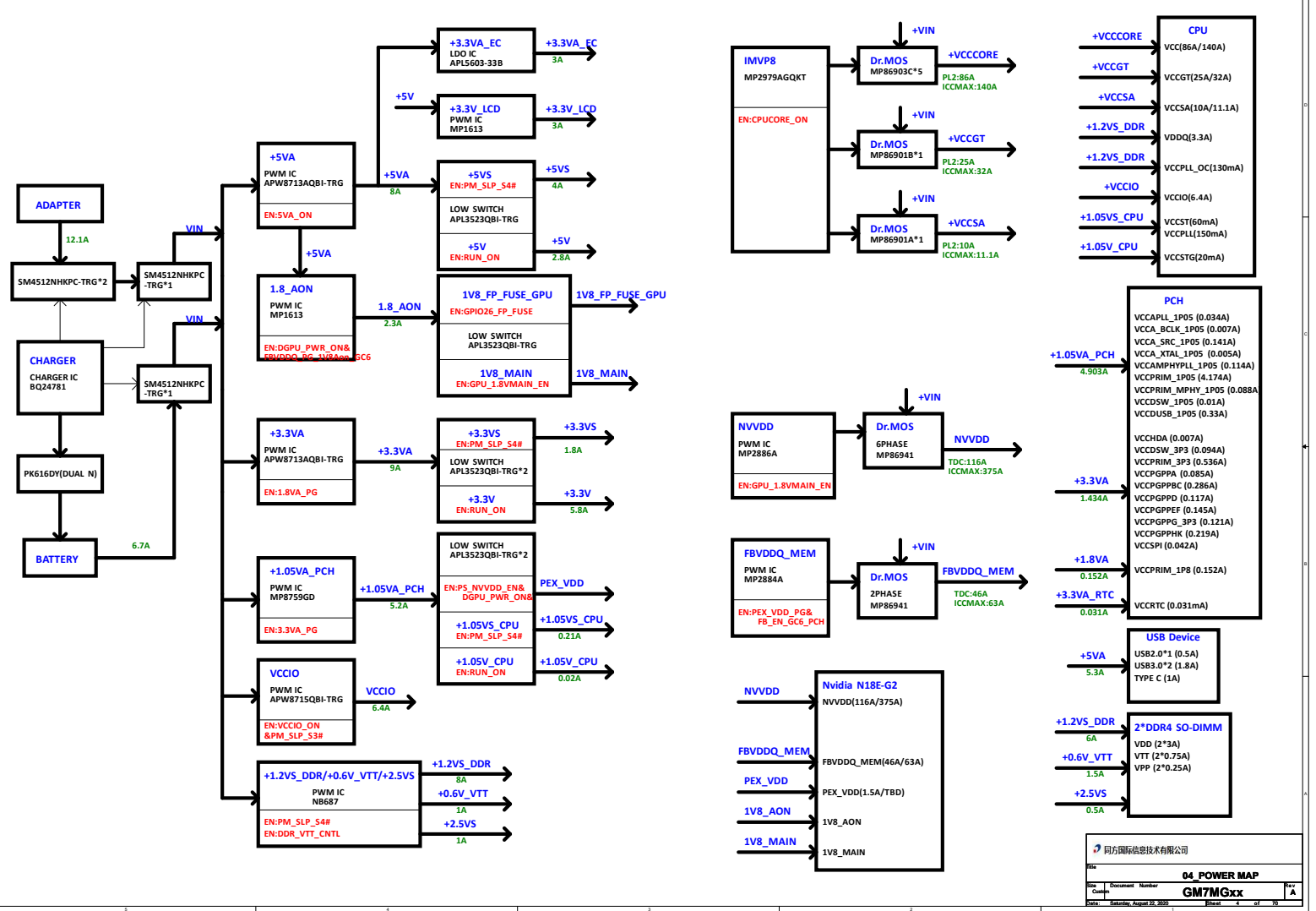


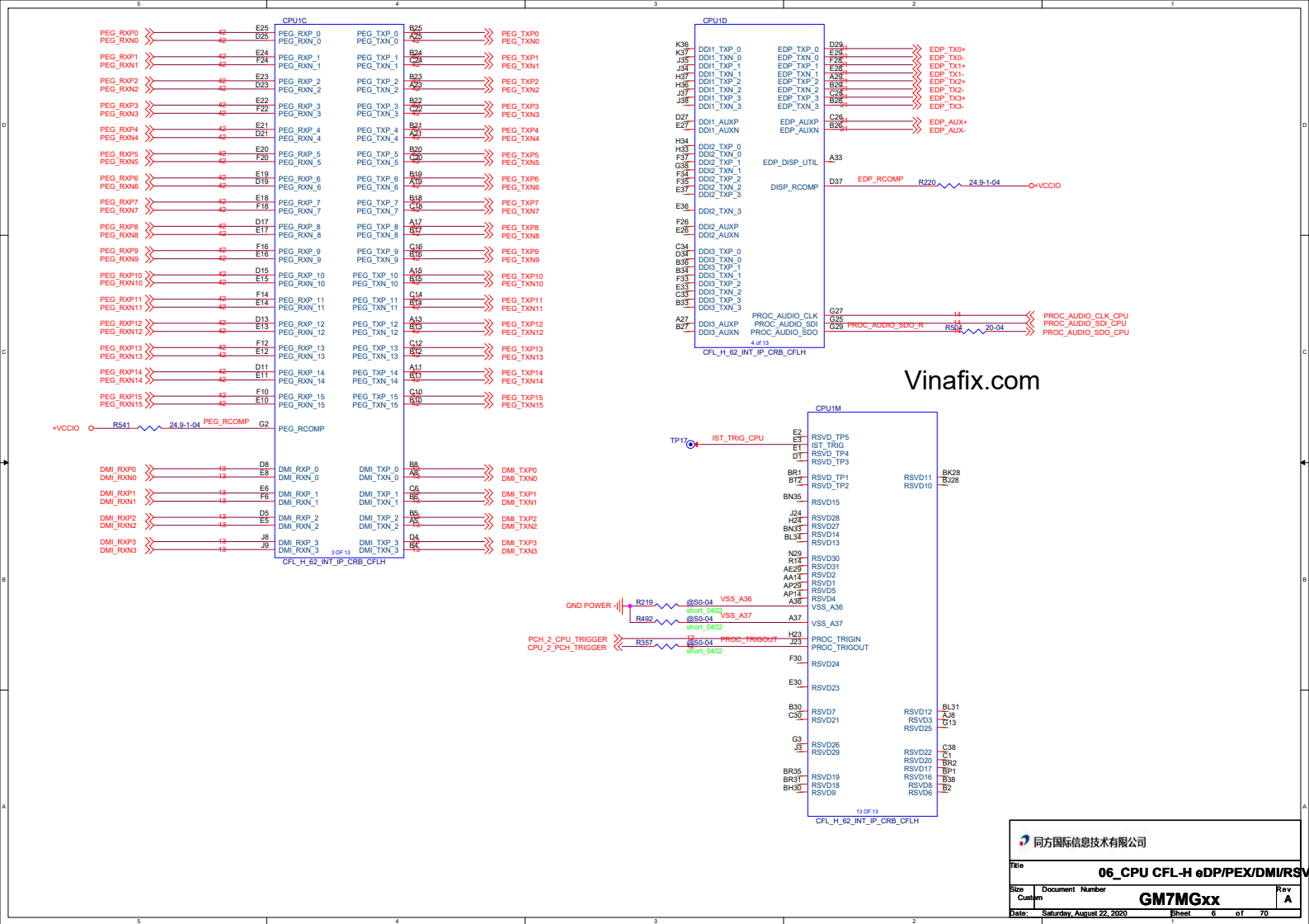
POWER ON SEQUENCE



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Rev	03_POWER SEQUENCE		
Doc	Document Number	GM7MGxx	
Chg	Change	Date	Wednesday, August 22, 2018
Rev		3	01
		A	

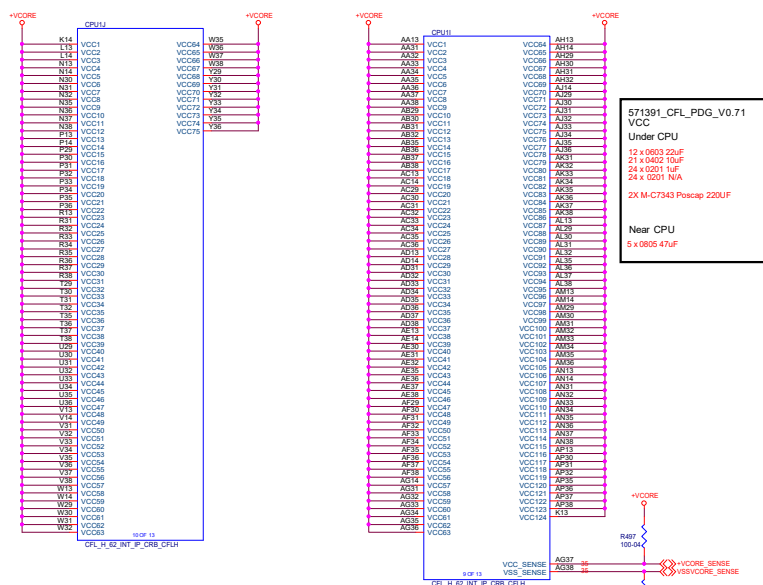




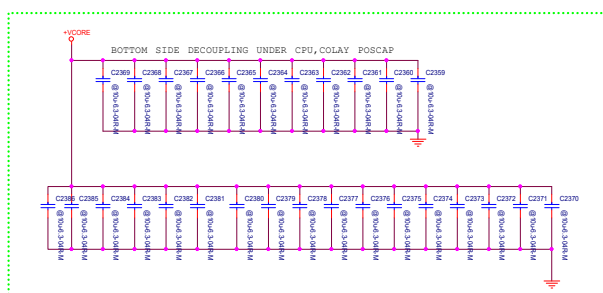
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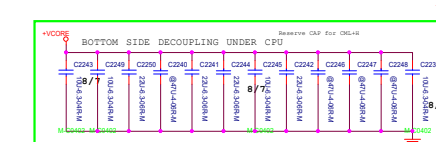
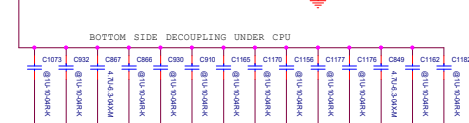
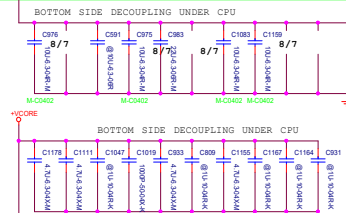
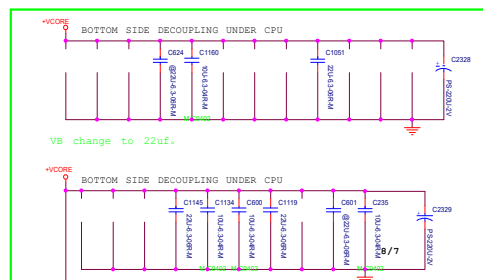
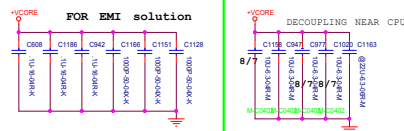
Title			06_CPU CFL-H eDP/PEX/DMI/RSV
Size	Document Number	GM7MGxx	
Customer			Rev A
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FOR EMI solution



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FOR EMI solution

611586_CML_H_PDG_Rev0p9

VCCGT
Bulk Decoupling Example
2 x 220uF

Processor Decoupling Requirements

3x 47uF 0805
7x 22uF 0603
10 10 5 0402

10x 10uF 0402
12x 1uF 0201/0402

VccGT

Page 9 : $22u \cdot 20 + 4.7u \cdot 12 =$
 Page 36 : $22u \cdot 6 + 330u \cdot 2 = 792u$
 Total : $1200 \cdot 4u + 5 \cdot (page) = 947 \cdot 5$

total : 1288.40F (spec : 847UF)



611586_CML_H_PDG_Rev0p9
VccIO
Bulk Decoupling Example
Processor Decoupling Requirements

611586_CML_H_PDG_Rev0p9
VccSA
Bulk Decoupling Example
Processor Decoupling Requirements

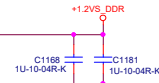
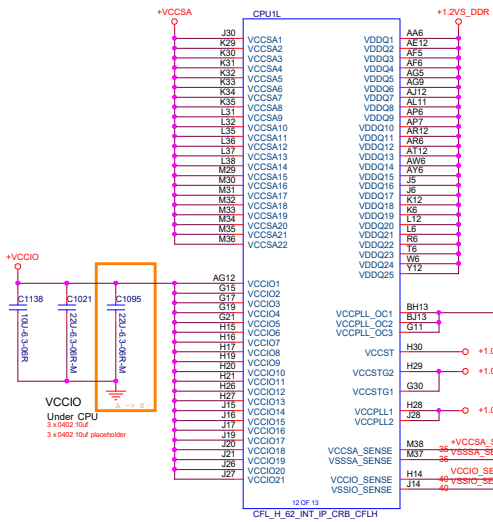
611586_CML_H_PDG_Rev0p9
Processor Decoupling Requirements
VDDQ
VccSTG
VccPLL
VccPLL_OC

VccIO
Page 10 : 22u*2 +10*1 = 54uF
Page 40 : 22u*4 =88uF
Total : 142uF (CML-H spec : 124uF)

VccSA
Page 10 : 47u + 12 =564uF
Page 36 : 22u + 4 =88uF
Total : 654uF (spec : 523uF)

VDDQ
Page 10 : 22u * 15 =330uF
Total : 330uF (spec : 198uF)

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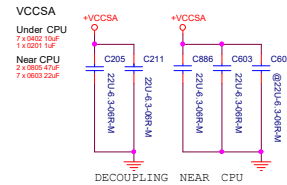
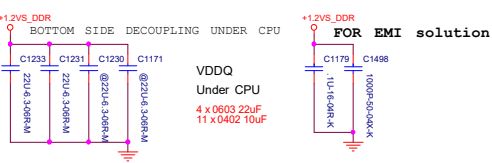
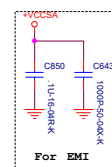
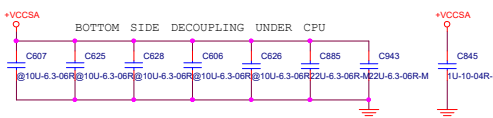
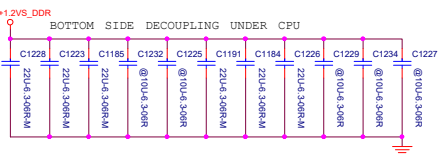
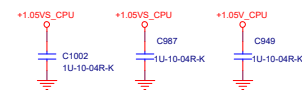
VCCST
Under CPU
1 x 0201 1uF
VCCSTG
Under CPU
1 x 0201 1uF
VCCPLL
Under CPU
1 x 0201 1uF
VCCPLL_OC
Under CPU
2 x 0201 1uF

VCCPLL_OC:
CPU digital PLL power rails
VCCPLL:
CPU PLL power rails

VCCSTG:
Sustain voltage for processor
in Standby modes
VCCSTG:
Gated version of VCCST

(1)VCCPLL is allowed to be OFF in S3,
but it is generally assumed to be ON
since it is powered from the same
source as VCCST.

(2) VCCPLL_OC is allowed to be turned
off during S3 if it is not powered
directly from VDDQ



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Title 10_CPU CFL-H VCCSA/VCCIO/VDDQ			
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CPUIF			AK4		
A10	VSS_1	VSS_82	AL10	VSS_83	
A12	VSS_3	VSS_84	AL12	VSS_85	
A16	VSS_4	VSS_86	AL14	VSS_87	
A20	VSS_5	VSS_88	AL30	VSS_89	
A22	VSS_6	VSS_90	AL32	VSS_91	
A24	VSS_7	VSS_92	AL4	VSS_93	
A26	VSS_8	VSS_94	AL6	VSS_95	
A28	VSS_9	VSS_96	AL8	VSS_97	
A30	VSS_10	VSS_98	AL9	VSS_99	
A6	VSS_11	VSS_100	AM1	VSS_101	
A12	VSS_12	VSS_102	AM12	VSS_103	
AA20	VSS_13	VSS_104	AM2	VSS_105	
AA30	VSS_14	VSS_106	AM3	VSS_107	
AB33	VSS_15	VSS_108	AM39	VSS_109	
AB34	VSS_16	VSS_110	AM6	VSS_111	
AB6	VSS_17	VSS_112	AM6	VSS_113	
AC1	VSS_18	VSS_114	AN12	VSS_115	
AC12	VSS_19	VSS_116	AN20	VSS_117	
AC2	VSS_20	VSS_118	AN30	VSS_119	
AC3	VSS_21	VSS_120	AN5	VSS_121	
AC31	VSS_22	VSS_122	AN6	VSS_123	
AC38	VSS_23	VSS_124	AP10	VSS_125	
AC4	VSS_24	VSS_126	AP11	VSS_127	
AC5	VSS_25	VSS_128	AP12	VSS_129	
AC6	VSS_26	VSS_130	AP33	VSS_131	
AD10	VSS_27	VSS_132	AP34	VSS_133	
AD11	VSS_28	VSS_134	AP8	VSS_135	
AD20	VSS_29	VSS_136	AP9	VSS_137	
AD30	VSS_30	VSS_138	AP1	VSS_139	
AD31	VSS_31	VSS_140	AR1	VSS_141	
AD5	VSS_32	VSS_142	AR13	VSS_143	
AD8	VSS_33	VSS_144	AR2	VSS_145	
AD9	VSS_34	VSS_146	AR29	VSS_147	
AE33	VSS_35	VSS_148	AR3	VSS_149	
AE34	VSS_36	VSS_150	AR30	VSS_151	
AE6	VSS_37	VSS_152	AR31	VSS_153	
AF1	VSS_38	VSS_154	AR32	VSS_155	
AF12	VSS_39	VSS_156	AR33	VSS_157	
AF13	VSS_40	VSS_158	AR34	VSS_159	
AF14	VSS_41	VSS_160	AR35	VSS_161	
AF2	VSS_42	VSS_162	AR36	VSS_163	
AF3	VSS_43	VSS_164	AR37	VSS_165	
AF4	VSS_44	VSS_166	AR38	VSS_167	
AG10	VSS_45	VSS_168	AR4	VSS_169	
AG11	VSS_46	VSS_170	AR5	VSS_171	
AG13	VSS_47	VSS_172	AT20	VSS_173	
AG20	VSS_48	VSS_174	AT30	VSS_175	
AG30	VSS_49	VSS_176	AT6	VSS_177	
AG6	VSS_50	VSS_178	AT10	VSS_179	
AG7	VSS_51	VSS_180	AU10	VSS_181	
AG8	VSS_52	VSS_182	AU12	VSS_183	
AH12	VSS_53	VSS_184	AU33	VSS_185	
AH33	VSS_54	VSS_186	AU34	VSS_187	
AH34	VSS_55	VSS_188	AU6	VSS_189	
AH35	VSS_56	VSS_190	AU7	VSS_191	
AH36	VSS_57	VSS_192	AU8	VSS_193	
AH6	VSS_58	VSS_194	AU9	VSS_195	
AJ1	VSS_59	VSS_196	AV37	VSS_197	
AJ13	VSS_60	VSS_198	AV39	VSS_199	
AJ2	VSS_61	VSS_200	AW1	VSS_201	
AJ3	VSS_62	VSS_202	AW12	VSS_203	
AJ38	VSS_63	VSS_204	AW2	VSS_205	
AJ4	VSS_64	VSS_206	AW29	VSS_207	
AJ5	VSS_65	VSS_208	AW3	VSS_209	
AJ6	VSS_66	VSS_210	AW30	VSS_211	
AJ6	VSS_67	VSS_212	AW4	VSS_213	
W4	VSS_68	VSS_214	W6	VSS_215	
W5	VSS_69	VSS_216	W12	VSS_217	
W6	VSS_70	VSS_218	W2	VSS_219	
Y10	VSS_71	VSS_220	W3	VSS_221	
Y11	VSS_72	VSS_222	W33	VSS_223	
Y14	VSS_73	VSS_224	W34	VSS_225	
Y37	VSS_74	VSS_226			
Y4	VSS_75	VSS_228			
Y8	VSS_76	VSS_230			
Y7	VSS_77	VSS_232			
Y9	VSS_78	VSS_234			
AK29	VSS_79	VSS_236			
AK30	VSS_80	VSS_238			
	VSS_81	VSS_240			

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CFL_H_62_INT_IP_CRB_CFLH

CPUIG			BU15		
AW5	VSS_163	VSS_244	BU15	VSS_325	
AY3	VSS_164	VSS_245	B22	VSS_326	
AY34	VSS_165	VSS_246	B225	VSS_327	
BA10	VSS_166	VSS_247	B30	VSS_328	
BA11	VSS_167	VSS_248	B33	VSS_329	
BA12	VSS_168	VSS_249	B33	VSS_330	
BA12	VSS_169	VSS_250	B33	VSS_331	
BA37	VSS_170	VSS_251	B33	VSS_332	
B33	VSS_171	VSS_252	B34	VSS_333	
B46	VSS_172	VSS_253	B35	VSS_334	
B47	VSS_173	VSS_254	B36	VSS_335	
B47	VSS_174	VSS_255	B37	VSS_336	
B49	VSS_175	VSS_256	BK14	VSS_337	
B61	VSS_176	VSS_257	BK15	VSS_338	
BB12	VSS_177	VSS_258	BK16	VSS_339	
BB2	VSS_178	VSS_259	BK17	VSS_340	
BB29	VSS_179	VSS_260	BK25	VSS_341	
BB3	VSS_180	VSS_261	BK29	VSS_342	
BB3	VSS_181	VSS_262	BK29	VSS_343	
BB4	VSS_182	VSS_263	BL13	VSS_344	
BB5	VSS_183	VSS_264	BL14	VSS_345	
BB6	VSS_184	VSS_265	BL18	VSS_346	
BC12	VSS_185	VSS_266	BL19	VSS_347	
BC13	VSS_186	VSS_267	BL20	VSS_348	
BC14	VSS_187	VSS_268	BL21	VSS_349	
BC33	VSS_188	VSS_269	BL22	VSS_350	
BC34	VSS_189	VSS_270	BL23	VSS_351	
BC6	VSS_190	VSS_271	BL33	VSS_352	
BC6	VSS_191	VSS_272	BL36	VSS_353	
BD10	VSS_192	VSS_273	BL36	VSS_354	
BD12	VSS_193	VSS_274	BL6	VSS_355	
BD13	VSS_194	VSS_275	BL11	VSS_356	
BD3	VSS_195	VSS_276	BM12	VSS_357	
BD6	VSS_196	VSS_277	BM13	VSS_358	
BD7	VSS_197	VSS_278	BM14	VSS_359	
BD9	VSS_198	VSS_279	BM18	VSS_360	
BE1	VSS_199	VSS_280	BM2	VSS_361	
BE2	VSS_200	VSS_281	BM21	VSS_362	
BE29	VSS_201	VSS_282	BM22	VSS_363	
BE3	VSS_202	VSS_283	BM23	VSS_364	
BE30	VSS_203	VSS_284	BM24	VSS_365	
BE3	VSS_204	VSS_285	BM25	VSS_366	
BE4	VSS_205	VSS_286	BM26	VSS_367	
BE6	VSS_206	VSS_287	BM27	VSS_368	
BE7	VSS_207	VSS_288	BM28	VSS_369	
BF33	VSS_208	VSS_289	BM29	VSS_370	
BF34	VSS_209	VSS_290	BM3	VSS_371	
BF6	VSS_210	VSS_291	BM33	VSS_372	
BG12	VSS_211	VSS_292	BM35	VSS_373	
BG13	VSS_212	VSS_293	BM38	VSS_374	
BG14	VSS_213	VSS_294	BM5	VSS_375	
BG37	VSS_214	VSS_295	BM6	VSS_376	
BG38	VSS_215	VSS_296	BM7	VSS_377	
BG6	VSS_216	VSS_297	BM8	VSS_378	
BH1	VSS_217	VSS_298	BM9	VSS_379	
BH10	VSS_218	VSS_299	BN12	VSS_380	
BH11	VSS_219	VSS_300	BN14	VSS_381	
BH12	VSS_220	VSS_301	BN16	VSS_382	
BH14	VSS_221	VSS_302	BN19	VSS_383	
BH2	VSS_222	VSS_303	BN2	VSS_384	
BH3	VSS_223	VSS_304	BN20	VSS_385	
BH4	VSS_224	VSS_305	BN21	VSS_386	
BH5	VSS_225	VSS_306	BN24	VSS_387	
BH6	VSS_226	VSS_307	BN29	VSS_388	
BH7	VSS_227	VSS_308	BN30	VSS_389	
BH8	VSS_228	VSS_309	BN31	VSS_390	
BH9	VSS_229	VSS_310	BN34	VSS_391	
Y2	VSS_230	VSS_311	P6	VSS_392	
Y3	VSS_231	VSS_312	P6	VSS_393	
Y33	VSS_232	VSS_313	P12	VSS_394	
Y34	VSS_233	VSS_314	P26	VSS_395	
Y4	VSS_234	VSS_315	AY14	VSS_396	
Y5	VSS_235	VSS_316	AY14	VSS_397	
Y6	VSS_236	VSS_317	AY14	VSS_398	
Y7	VSS_237	VSS_318	AY14	VSS_399	
Y8	VSS_238	VSS_319	AY14	VSS_400	
Y9	VSS_239	VSS_320	AY14	VSS_401	
Y38	VSS_240	VSS_321	AY14	VSS_402	
Y39	VSS_241	VSS_322	AY14	VSS_403	
Y40	VSS_242	VSS_323	AY14	VSS_404	
Y41	VSS_243	VSS_324	AY14	VSS_405	

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CFL_H_62_INT_IP_CRB_CFLH

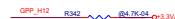
CPU1H			
BN4	VSS_325	VSS_409	F15
BN7	VSS_327	VSS_411	F17
BP12	VSS_328	VSS_412	F19
BP18	VSS_328	VSS_413	F21
BP21	VSS_329	VSS_414	F22
BP24	VSS_330	VSS_415	F23
BP25	VSS_331	VSS_416	F27
BP26	VSS_332	VSS_416	F3
BP29	VSS_333	VSS_417	F31
BP30	VSS_334	VSS_418	F33
BP33	VSS_335	VSS_419	F36
BP7	VSS_336	VSS_420	F4
BR12	VSS_337	VSS_421	F5
BR14	VSS_338	VSS_422	F6
BR18	VSS_339	VSS_423	F7
BR24	VSS_340	VSS_424	F8
BR25	VSS_341	VSS_425	F9
BR26	VSS_342	VSS_426	F10
BR29	VSS_343	VSS_427	F11
BR34	VSS_344	VSS_428	F12
BR36	VSS_345	VSS_429	F13
BR7	VSS_346	VSS_430	F14
BT12	VSS_348	VSS_432	G24
BT14	VSS_349	VSS_433	G25
BT18	VSS_350	VSS_434	G26
BT21	VSS_351	VSS_435	G27
BT24	VSS_352	VSS_436	G4
BT25	VSS_353	VSS_437	G6
BT26	VSS_354	VSS_438	G7
BT29	VSS_355	VSS_439	G8
BT30	VSS_356	VSS_440	G9
BT33	VSS_357	VSS_441	H11
BT7	VSS_358	VSS_442	H12
C17	VSS_359	VSS_443	H13
C19	VSS_360	VSS_444	H25
C21	VSS_361	VSS_445	H26
C23	VSS_362	VSS_446	H27
C25	VSS_363	VSS_447	H30
C27	VSS_364	VSS_448	H35
C29	VSS_365	VSS_449	H38
C31	VSS_366	VSS_450	J25
C37	VSS_367	VSS_451	J27
C5	VSS_368	VSS_452	J33
C6	VSS_369	VSS_453	J36
C8	VSS_370	VSS_454	K3
D10	VSS_371	VSS_455	K7
D12	VSS_372	VSS_456	K10
D14	VSS_373	VSS_457	K11
D16	VSS_374	VSS_458	K2
D18	VSS_375	VSS_459	K3
D20	VSS_376	VSS_460	K4
D22	VSS_377	VSS_461	K5
D24	VSS_378	VSS_462	K6
D26	VSS_379	VSS_463	K7
D28	VSS_380	VSS_464	K8
D3	VSS_381	VSS_465	K9
D30	VSS_382	VSS_466	L29
D33	VSS_383	VSS_467	L30
D6	VSS_384	VSS_468	L33
D9	VSS_385	VSS_469	L34
E34	VSS_386	VSS_470	L36
E35	VSS_387	VSS_471	L37
E38	VSS_388	VSS_472	M13
E4	VSS_389	VSS_473	M10
E9	VSS_390	VSS_474	N11
E29	VSS_391	VSS_475	N12
E30	VSS_392	VSS_476	N13
N33	VSS_393	VSS_477	B78
N34	VSS_394	VSS_478	B93
N6	VSS_395		AB9
N5	VSS_396		A3
N8	VSS_397	VSS_A3	A4
N9	VSS_398	VSS_A3	A4
N8	VSS_399	VSS_A4	A3
N10	VSS_400	VSS_A4	A3
P17	VSS_401	VSS_B37	BR38
P18	VSS_402	VSS_B37	BR38
M14	VSS_403	VSS_B73	B735
M6	VSS_404	VSS_B735	B736
M7	VSS_405	VSS_B735	B736
F11	VSS_406	VSS_B735	C14
F12	VSS_407	VSS_B735	C14
F13	VSS_408	VSS_D38	D38

of I3

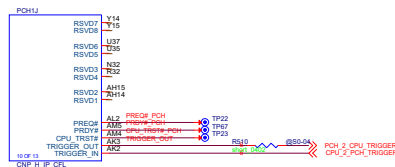
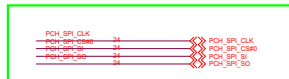
CPU_H_62_INT_INPR_CPLH_CPUH



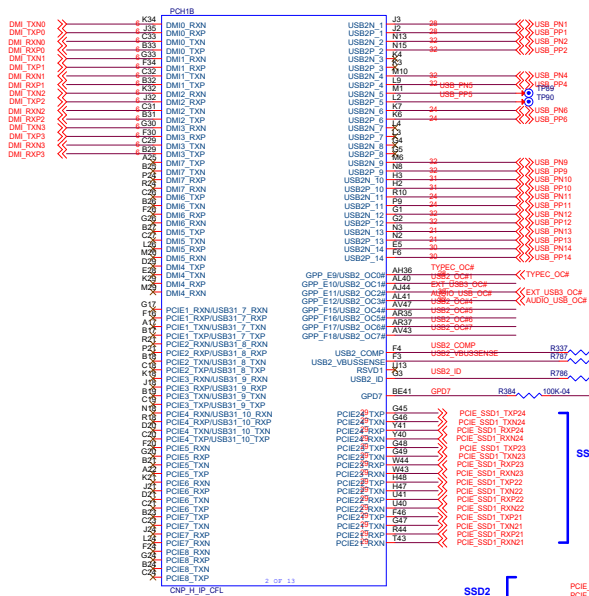
GPP_H12	eSPI Flash Sharing Mode
0	Master Attached Flash Sharing (MAFS) enabled (Default)
1	Slave Attached Flash Sharing (SAFS) enabled



to eSPI EC



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Title 12_PCH CFL-H SPI/DDI CTRL/RSVD	
Doc No C	Document Number GM7MGxx
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Rev A	



THUNDERBOLT

USB2.0 Configuration Table	
USB1	THUNDERBOLT
USB2	CardReader on USB3.0 DB
USB3	N/A
USB4	USB3.0 Port1 on USB3.0 DB
USB5	
USB6	ME Keyboard CONN
USB7	N/A
USB8	N/A
USB9	USB3.0 Port2 on USB3.0 DB
USB10	CNFP1: Finger Print
USB11	ME Keyboard CONN
USB12	USB2.0 PORT on Audio DB
USB13	Web Camera
USB14	Bluetooth

Only for CNP20

GP7 Reserved
External pull-up is required. Recommend 100K.

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

PCIe Configuration Table			
PCI9			
PCI10	SSD2		RST PCIe*4
PCI11			
PCI12			
PCI13	HDD		
PCI14	LAN		
PCI15	WLAN		
PCI16	N/A		
PCI17			
PCI18	Thunderbolt		PCI*4
PCI19			
PCI20			
PCI21			
PCI22	SSD1		RST PCIe*4
PCI23			
PCI24			

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

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Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

LAN

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Thunderbolt

SSD1

FB_EN_G0E_PCH

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Thunderbolt

SSD1

FB_EN_G0E_PCH

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FB_EN_G0E_PCH

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HDD

SSD2

Thunderbolt

SSD1

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LAN

HDD

SSD2

Thunderbolt

SSD1

FB_EN_G0E_PCH

SSD2

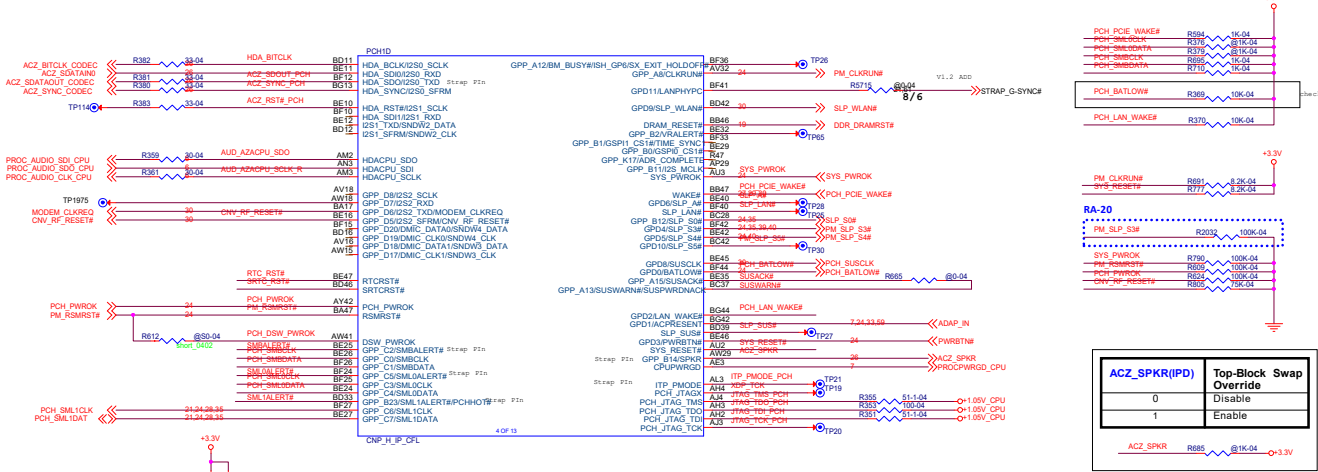
LAN

HDD

SSD2

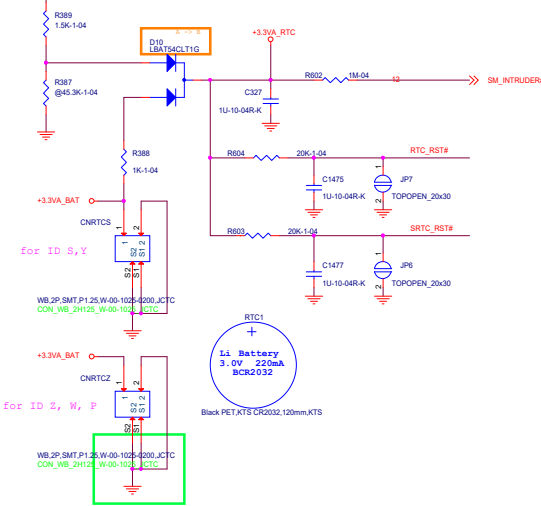
Thunderbolt

SSD1

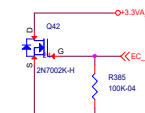


ACZ_SPKR(IPD)	Top-Block Swap Override
0	Disable
1	Enable


SUS Battery




CLEAR CMOS




Flash Descriptor Security Override	
0	SE Enable security (Default)
1	SE Disabled security

+3.3VA MELOCK# 


Intel ME Crypto Transport Layer Security Confidentiality (TLS)	
0	Disable (Default)
1	Enable

+3.3VA 

eSPI&LPC Select	
0	LPC (Default)
1	eSPI

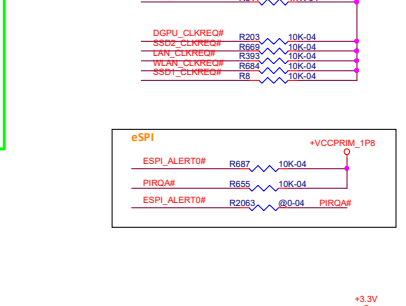
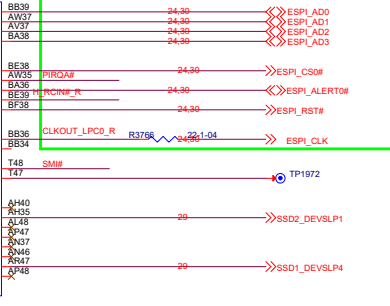
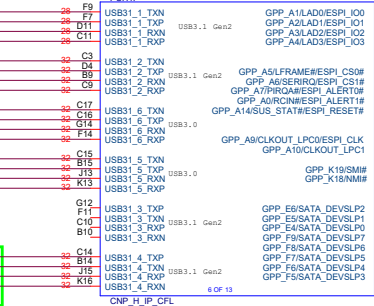
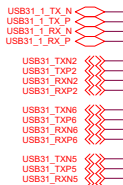
+3.3VA 

IntelR DCI-OOB	
0	Disable (Default)
1	Enable

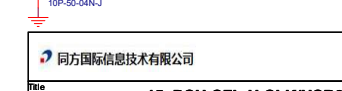
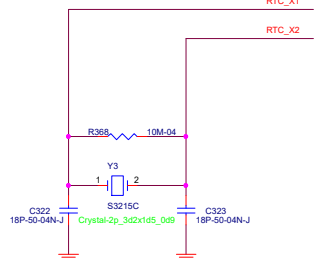
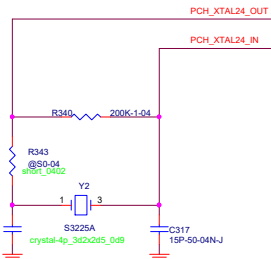
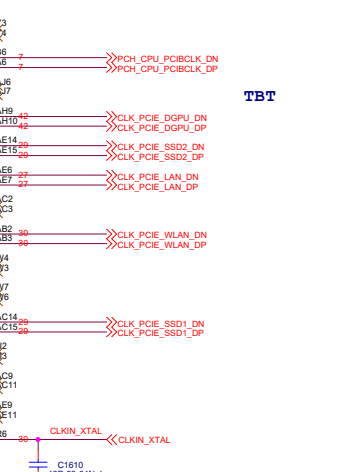
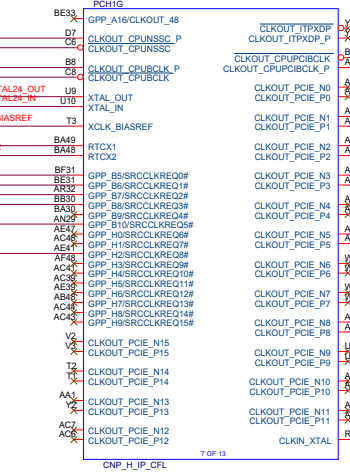
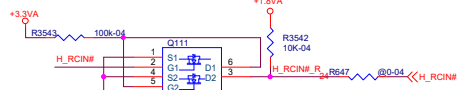
+3.3VA 

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Type-C
USB3.1 SD
USB3.1 USB DB
USB3.1 USB DB
USB3.1 Audio DB



USB3.0 Configuration Table	
USB3_1	N/A
USB3_2	Card Reader
USB3_3	N/A
USB3_4	USB3.1 Port Audio BD
USB3_5	USB3.0 Port1 USB DB
USB3_6	USB3.0 Port2 USB DB
USB3_7	N/A
USB3_8	N/A
USB3_9	No Function
USB3_10	No Function



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15_PCH CFL-H CLK/USB3/LPC

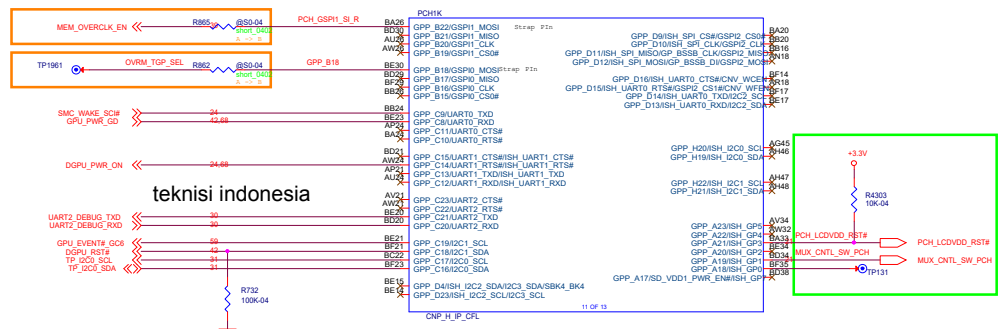
Size: Custom Document Number: GM7MGxx Rev: A

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GPP_B22/GSP11_MOSI(IPD)	Boot BIOS Destination
0	SPI (Default)
1	LPC



GPP_B18/GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable



CNV_BRI_DT (IPD)	XTAL Frequency Select
0	38.4MHz XTAL frequency
1	24MHz XTAL frequency (Default)

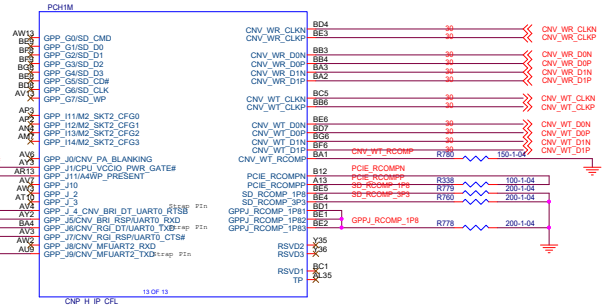


CNV_RGI_DT	M.2 CNV Mode Select
0	Integrated CNVi enable
1	Integrated CNVi disable



Close to CNVi module

GPP_J9	VCCPSPI Rail select
0	VCCSPI is connected to 3.3V
1	VCCSPI is connected to 1.8V

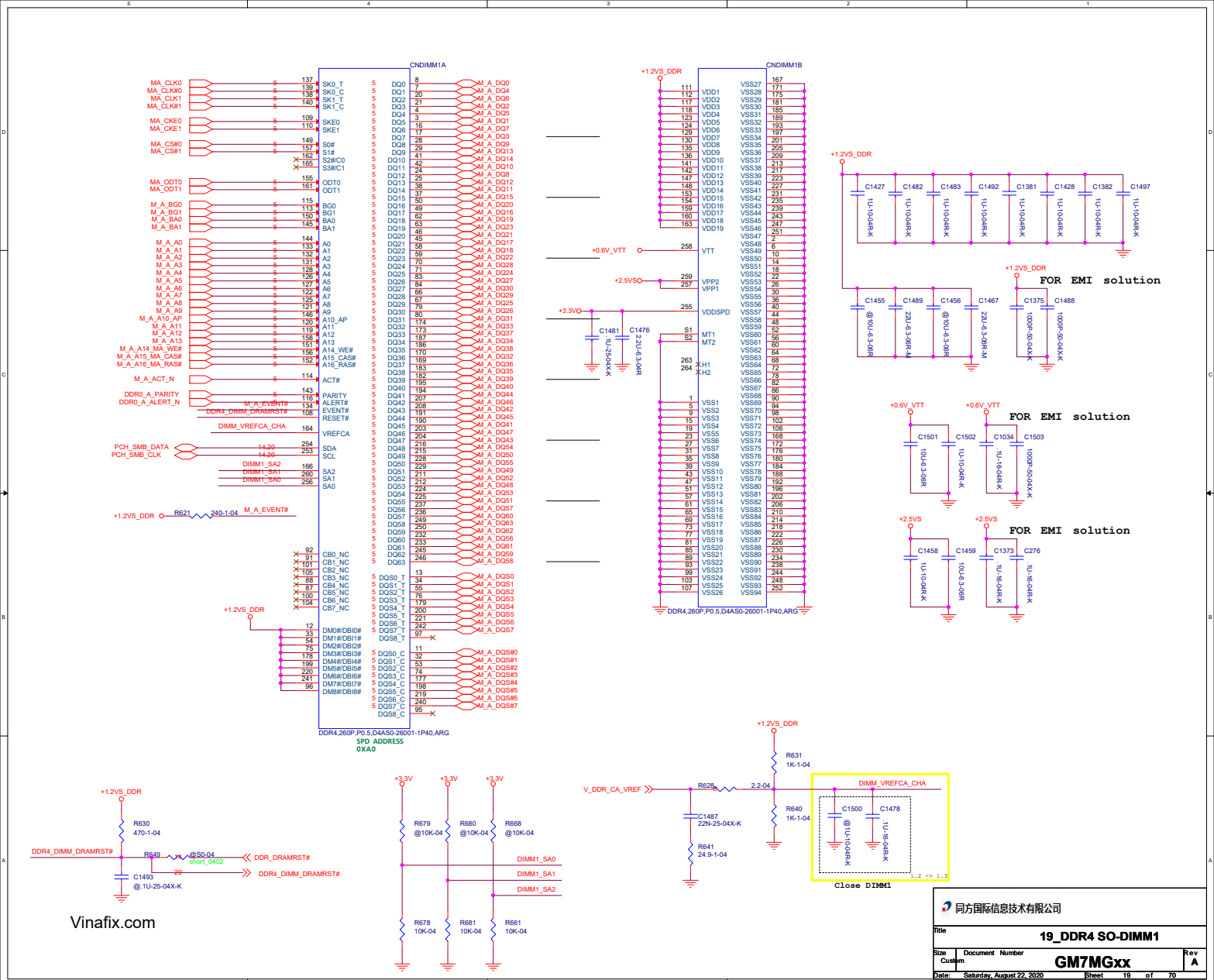


PCH11		
A2	VSS_1	AL12
A28	VSS_2	AL17
A3	VSS_3	AL21
A33	VSS_4	AL24
A37	VSS_5	AL26
A4	VSS_6	AL29
A45	VSS_7	AL33
A46	VSS_8	AL38
A47	VSS_9	AM1
A48	VSS_10	AM18
A5	VSS_11	AM32
A8	VSS_12	AM49
AA19	VSS_13	AN12
AA20	VSS_14	AN34
AA25	VSS_15	AN38
AA27	VSS_16	AP4
AA38	VSS_17	AP46
AA39	VSS_18	AR12
AA49	VSS_19	AR16
AA5	VSS_20	AR34
AB19	VSS_21	AR38
AB25	VSS_22	AT1
AB31	VSS_23	AT18
AC12	VSS_24	AT26
AC17	VSS_25	AT29
AC33	VSS_26	AT32
AC38	VSS_27	AT34
AC4	VSS_28	AT45
AC46	VSS_29	AV11
AD1	VSS_30	AV17
AD19	VSS_31	AV39
AD2	VSS_32	AW10
AD22	VSS_33	AW4
AD25	VSS_34	AW46
AD49	VSS_35	AW49
AE12	VSS_36	BA1
AE33	VSS_37	BA4
AE38	VSS_38	BA9
AE4	VSS_39	BA12
AE46	VSS_40	BA4
AF22	VSS_41	BA9
AF25	VSS_42	BA14
AF28	VSS_43	BA44
AG1	VSS_44	BA5
AG22	VSS_45	BA8
AG23	VSS_46	BB41
AG25	VSS_47	BB43
AG27	VSS_48	BB9
AG28	VSS_49	BC10
AG30	VSS_50	BC13
AG48	VSS_51	BC15
AH12	VSS_52	BC19
AH17	VSS_53	BC24
AH3	VSS_54	BC26
AH38	VSS_55	BC31
AJ19	VSS_56	BC35
AJ20	VSS_57	BC40
AJ25	VSS_58	BC45
AJ27	VSS_59	BC5
AJ28	VSS_60	BD43
AJ30	VSS_61	BD44
AJ31	VSS_62	BF1
AK19	VSS_63	BF2
AK30	VSS_64	BF3
AK25	VSS_65	BF48
AK27	VSS_66	BF49
AK28	VSS_67	BG17
AK30	VSS_68	BG2
AK31	VSS_69	BG22
AK4	VSS_70	BG25
AK46	VSS_71	BG28
	VSS_72	

PCH1L		
BG3	VSS_145	M24
BG33	VSS_146	M32
BG37	VSS_147	M34
BG4	VSS_148	M49
BG48	VSS_149	M5
C12	VSS_150	N12
C25	VSS_151	N16
C30	VSS_152	N34
C4	VSS_153	N35
C48	VSS_154	N37
C5	VSS_155	N38
D12	VSS_156	P26
D19	VSS_157	P29
D30	VSS_158	P46
D33	VSS_159	P12
D8	VSS_160	R16
E10	VSS_161	R12
E13	VSS_162	R20
E15	VSS_163	R3
E17	VSS_164	R34
E19	VSS_165	R38
E22	VSS_166	R4
E24	VSS_167	R17
E26	VSS_168	R18
E31	VSS_169	R32
E33	VSS_170	T4
E35	VSS_172	T49
E40	VSS_173	T5
E42	VSS_174	T7
F41	VSS_175	U12
F43	VSS_176	U15
F47	VSS_177	U17
G44	VSS_178	U21
G8	VSS_179	U24
H5	VSS_180	U33
J10	VSS_181	U38
J25	VSS_182	V20
J29	VSS_183	V22
J4	VSS_184	V4
J40	VSS_185	V46
J46	VSS_186	W25
J47	VSS_187	W27
J48	VSS_188	W28
J9	VSS_189	W30
K11	VSS_190	Y10
K39	VSS_191	Y12
M10	VSS_192	Y17
M18	VSS_193	Y33
M21	VSS_194	Y38
	VSS_195	Y9

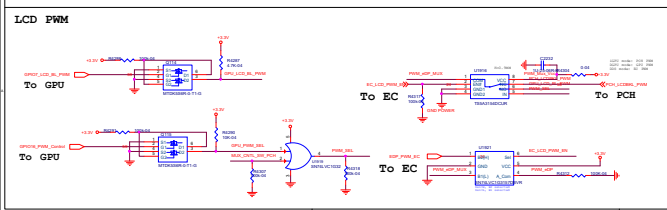
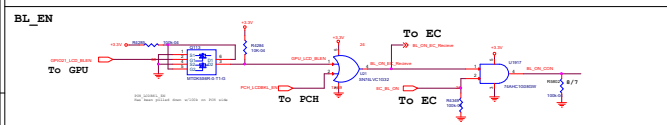
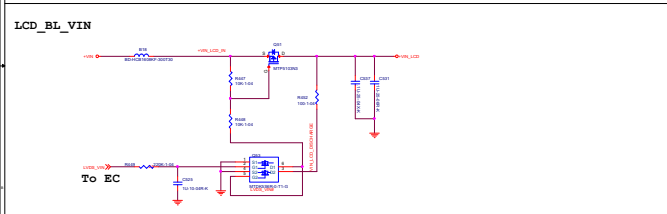
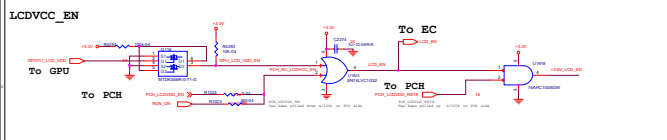
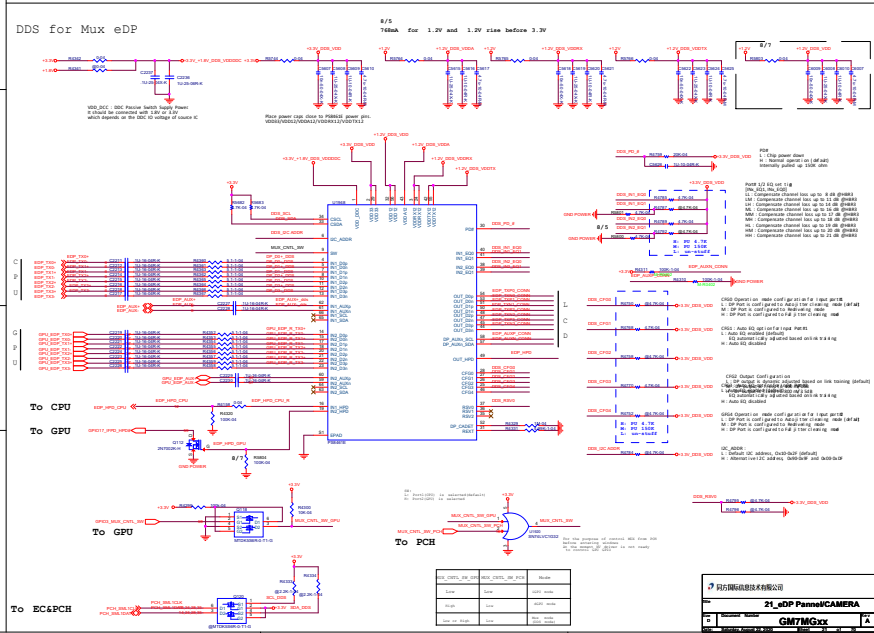
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CNP_H_IP_CFL

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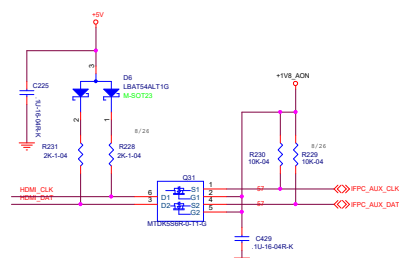
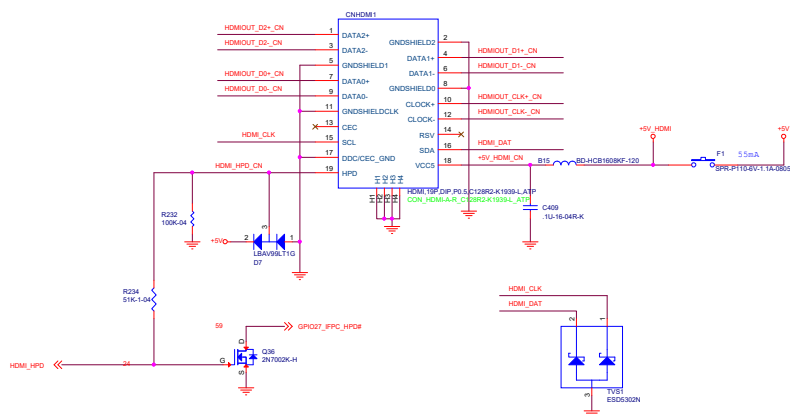
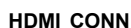


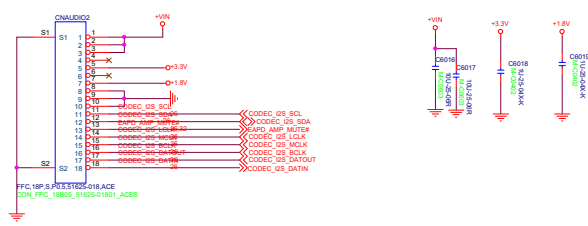
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HDMI R2.0	670MHz	NV Supported
HDMI R1.4	340MHz	Intel Supported






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同方国际信息技术有限公司			
Title			
23 Audio_Speaker Connector			
Rev	Document Number	Rev	
C		GM7MGxx	
Date		Revision	25 of 35
Schematic August 27, 2025			

5	4	3	2	1
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25 ME KB ESD			
Size A	Document Number		Rev A
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Date:	Saturday, August 22, 2020	Sheet	25 of 70

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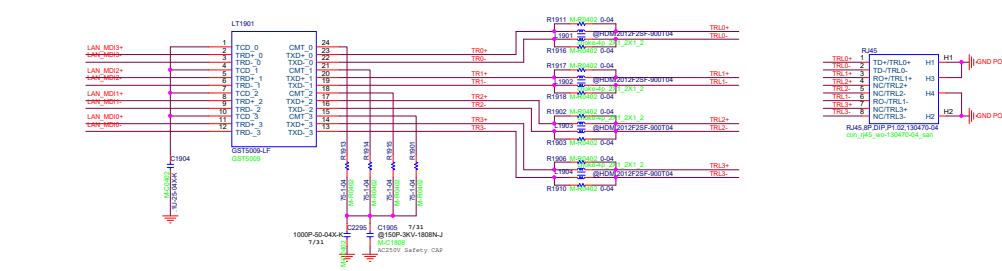
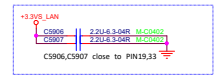
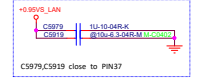
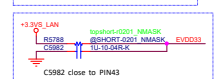
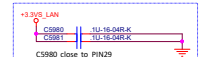
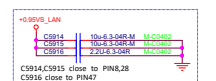
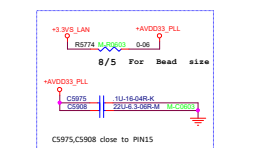
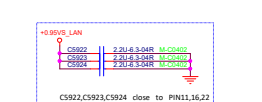
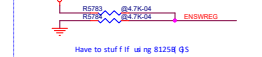
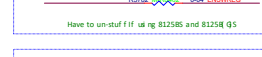
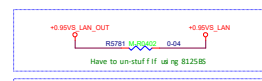
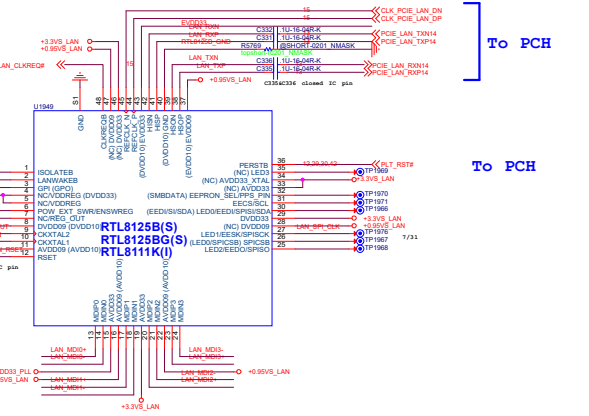
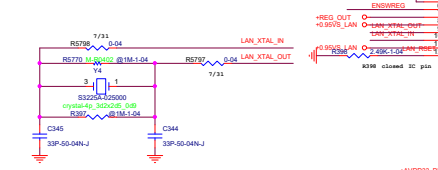
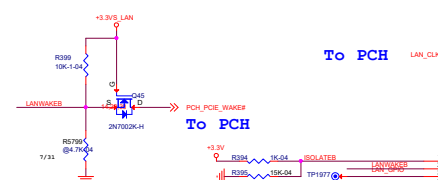
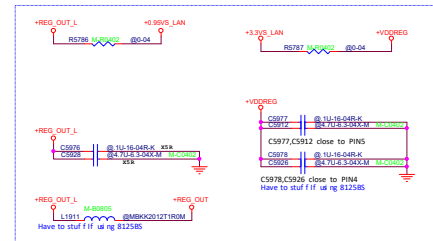
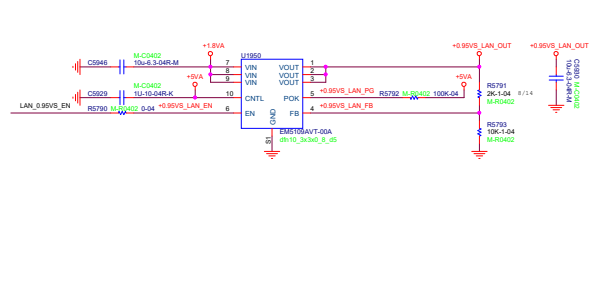
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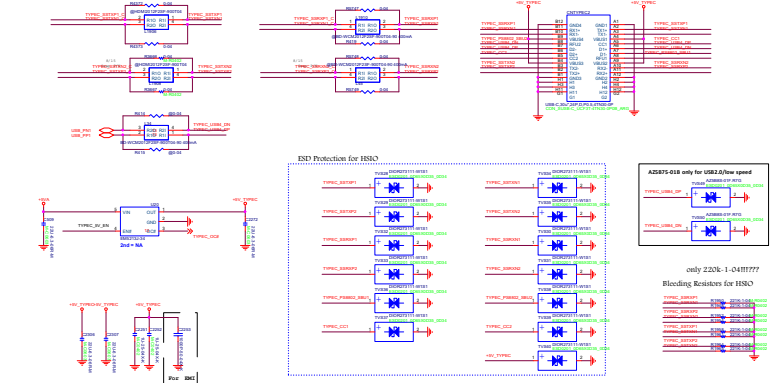
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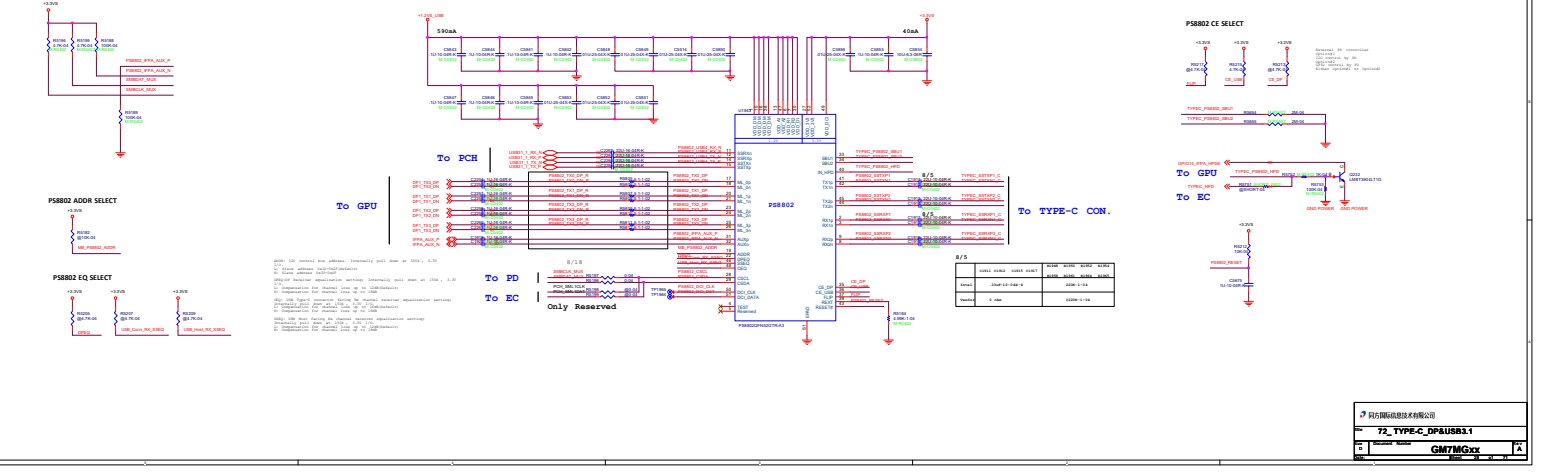
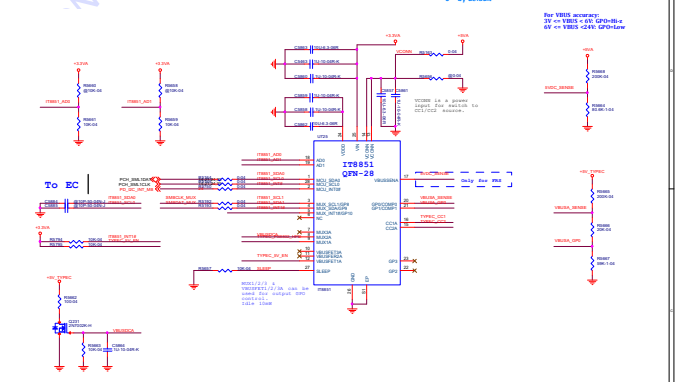
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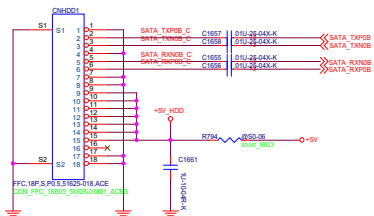
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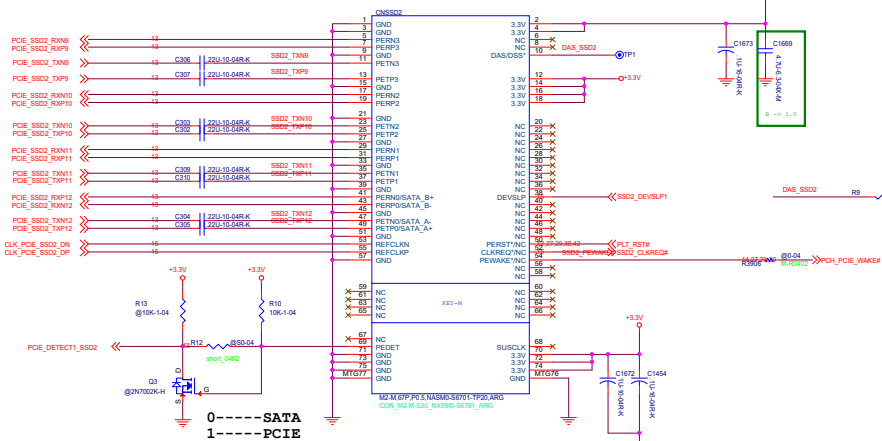
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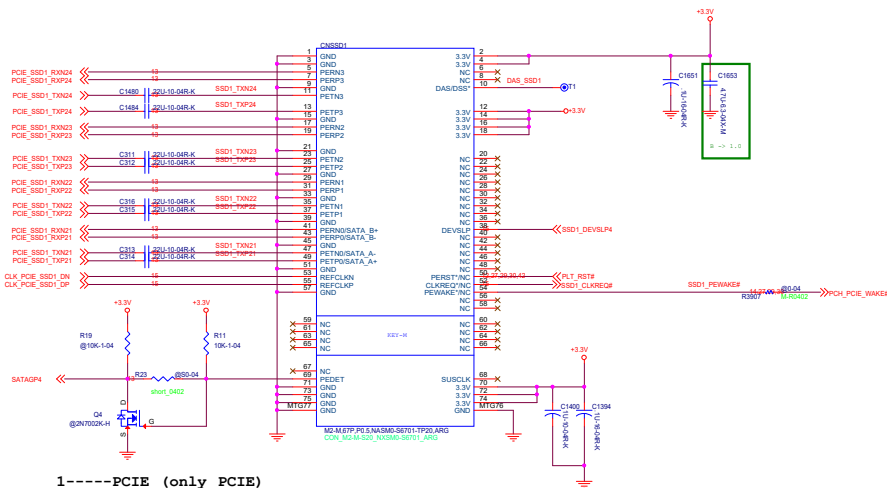
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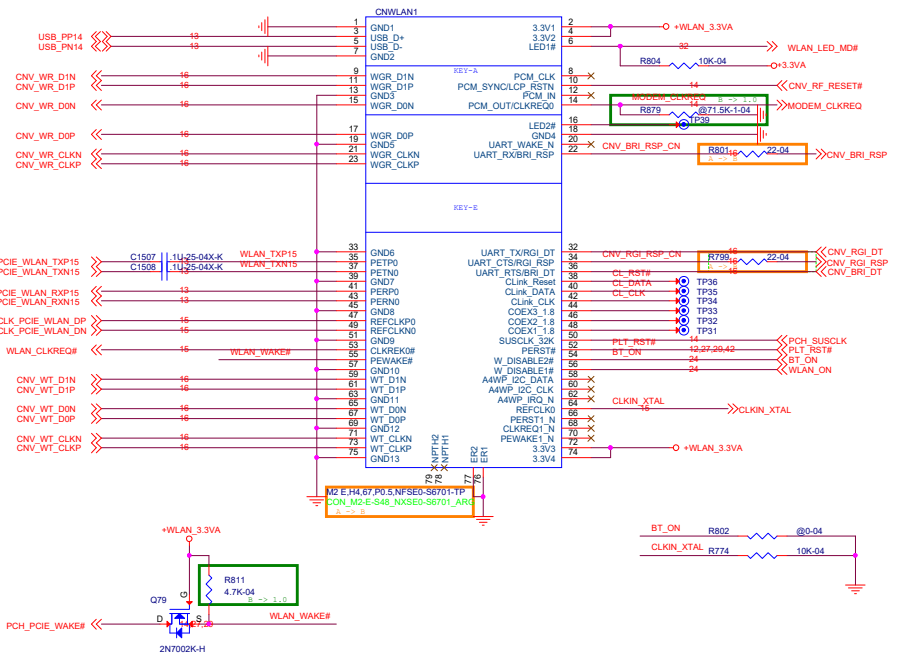
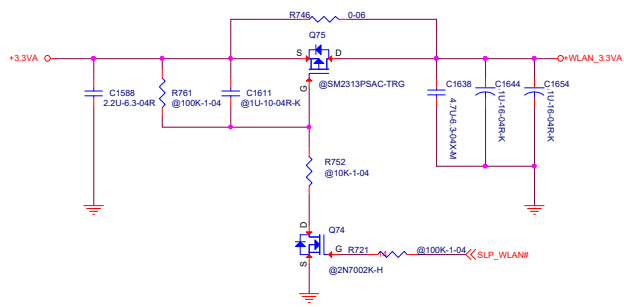
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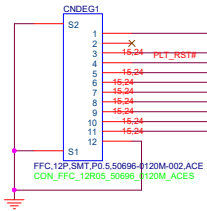
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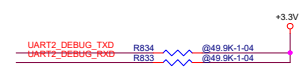
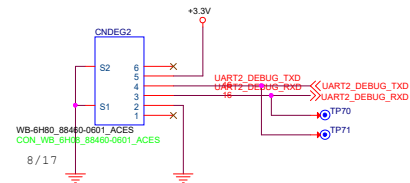
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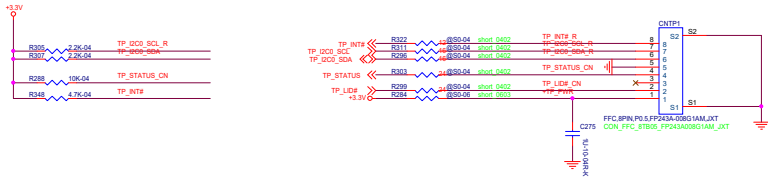
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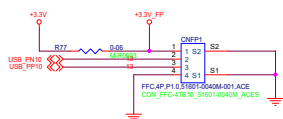
UART debug port



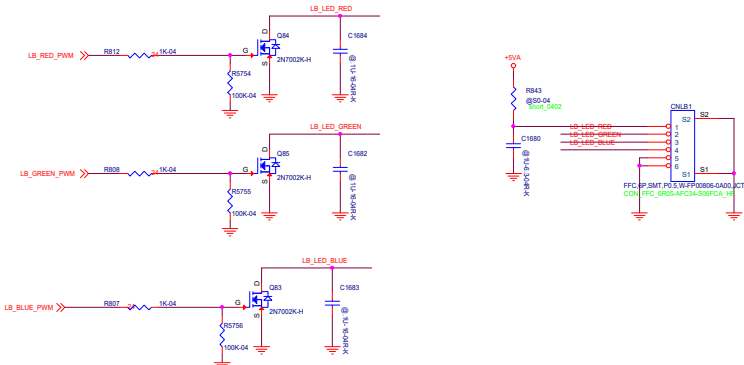
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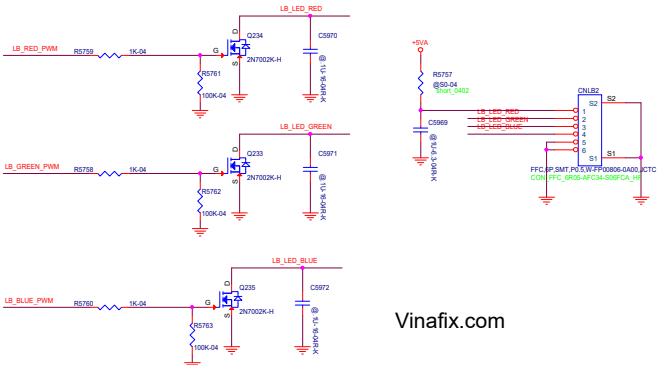
Finger Print



Light bar Control

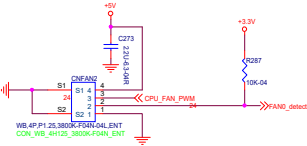


Keyboard Backlight Control

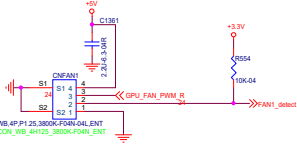


FAN CONTROLLER

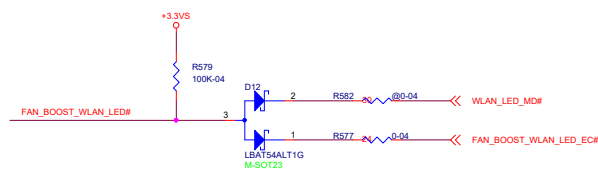
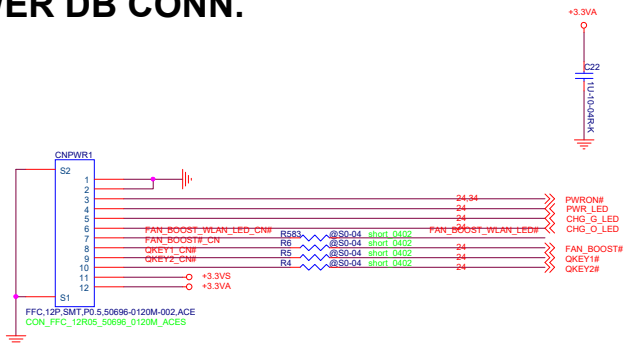
CPU FAN



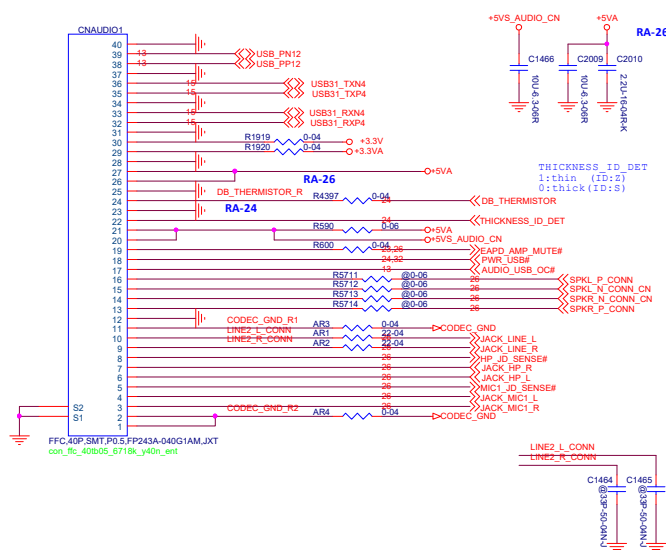
GPU FAN



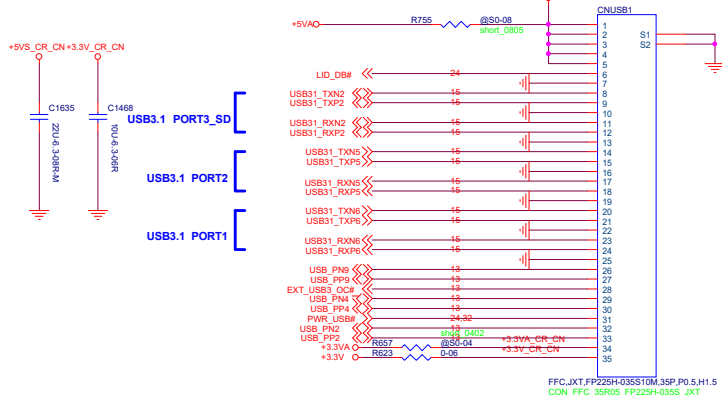
POWER DB CONN.



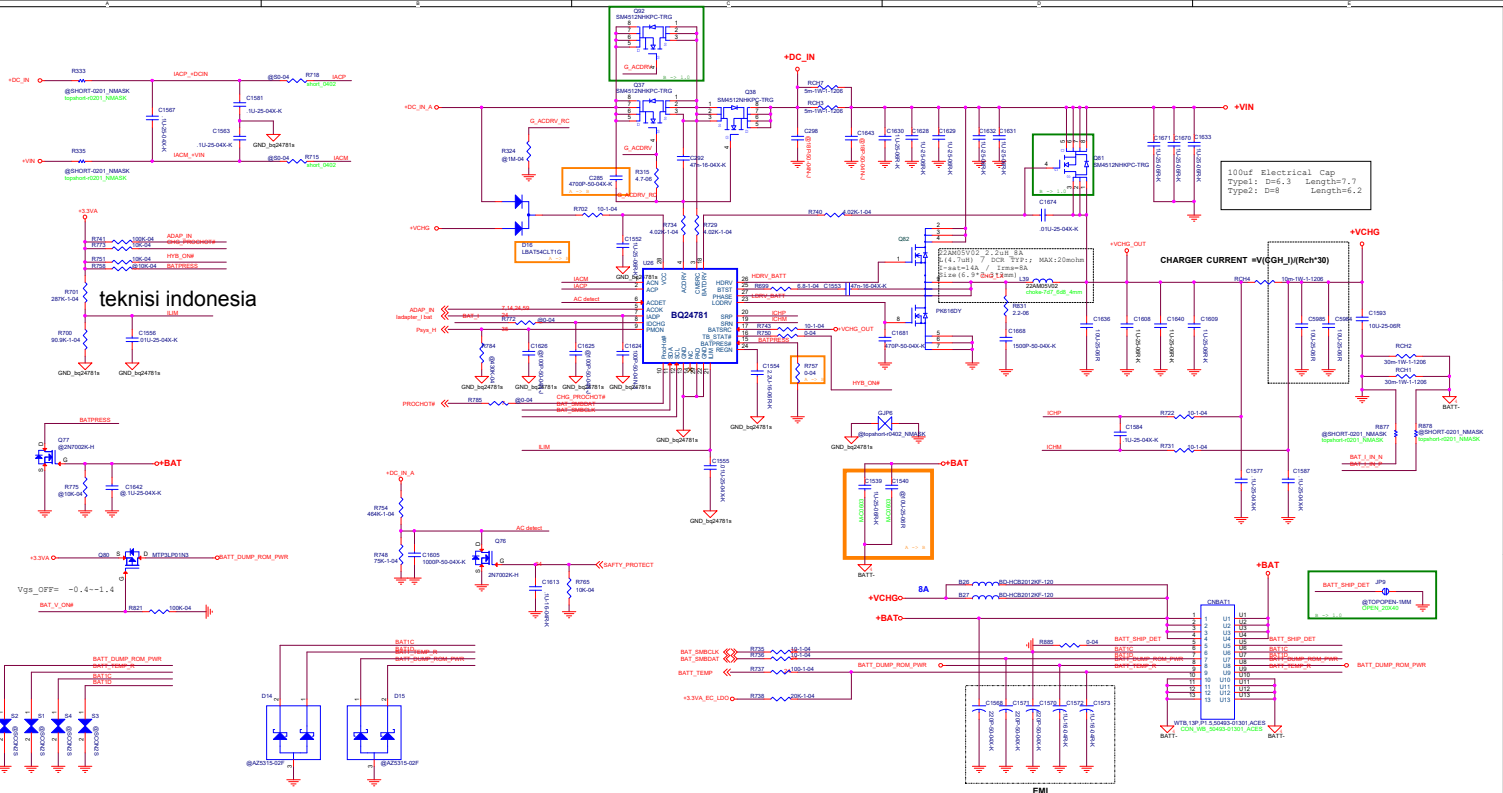
Audio&USB DB CONN.



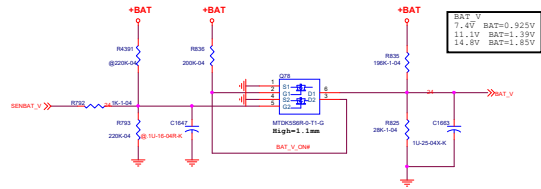
USB3.0 DB CONN.



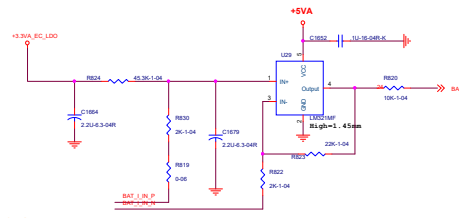
同方国际信息技术有限公司			
Title 32_PWR_DB/USB3.0 DB/Audio DB			
Size	Document Number	GM7MGxx	
Custom		Rev A	
Date:	Saturday, August 22, 2020	Sheet 32	of 70



Battery Voltage Detect



Battery Current Detect

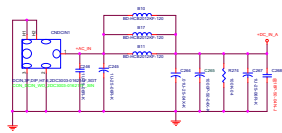


RCR1 //RCR2 =7.5mohm		RCR1 //RCR2 =15mohm	
BAT_I	ICRG (0.0842V/1A)	BAT_I	ICRG (0.1724V/1A)
1.8468V	2A	2.1840V	2A
1.7648V	1A	2.0192V	1A
1.7606V	0A	1.8468V	0A
1.6820V	-1A	1.6744V	-1A
1.5020V	-2A	1.3298V	-2A
1.3298V	-3A	1.0200V	-3A
1.1572V	-4A	0.6400V	-4A
0.9848V	-5A	0.2352V	-5A
0.8124V	-10A	0.1228V	-9A

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33_BATT IN/CHARGER(BQ24781)			
Doc	Doc Number	Rev	A
Comp			
GM7MGxx			
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+DC_IN

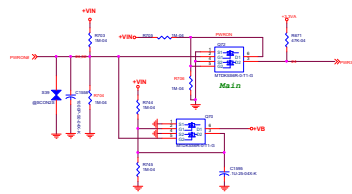


```

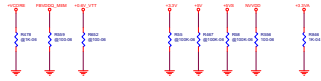
EMG20NP3V
ID=-11A   TC=100 deg
Ipulse=-72A
Avalanche=-10A
9watt 1ms
15Watt 0.1ms

```

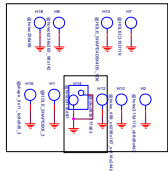
POWER SW



Discharge Resistor



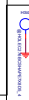
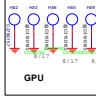
PCB HOLE



WLAN HOW



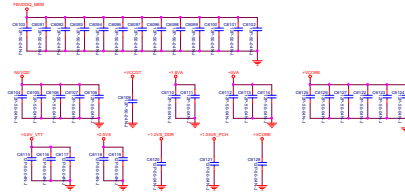
THERMAL HOLE



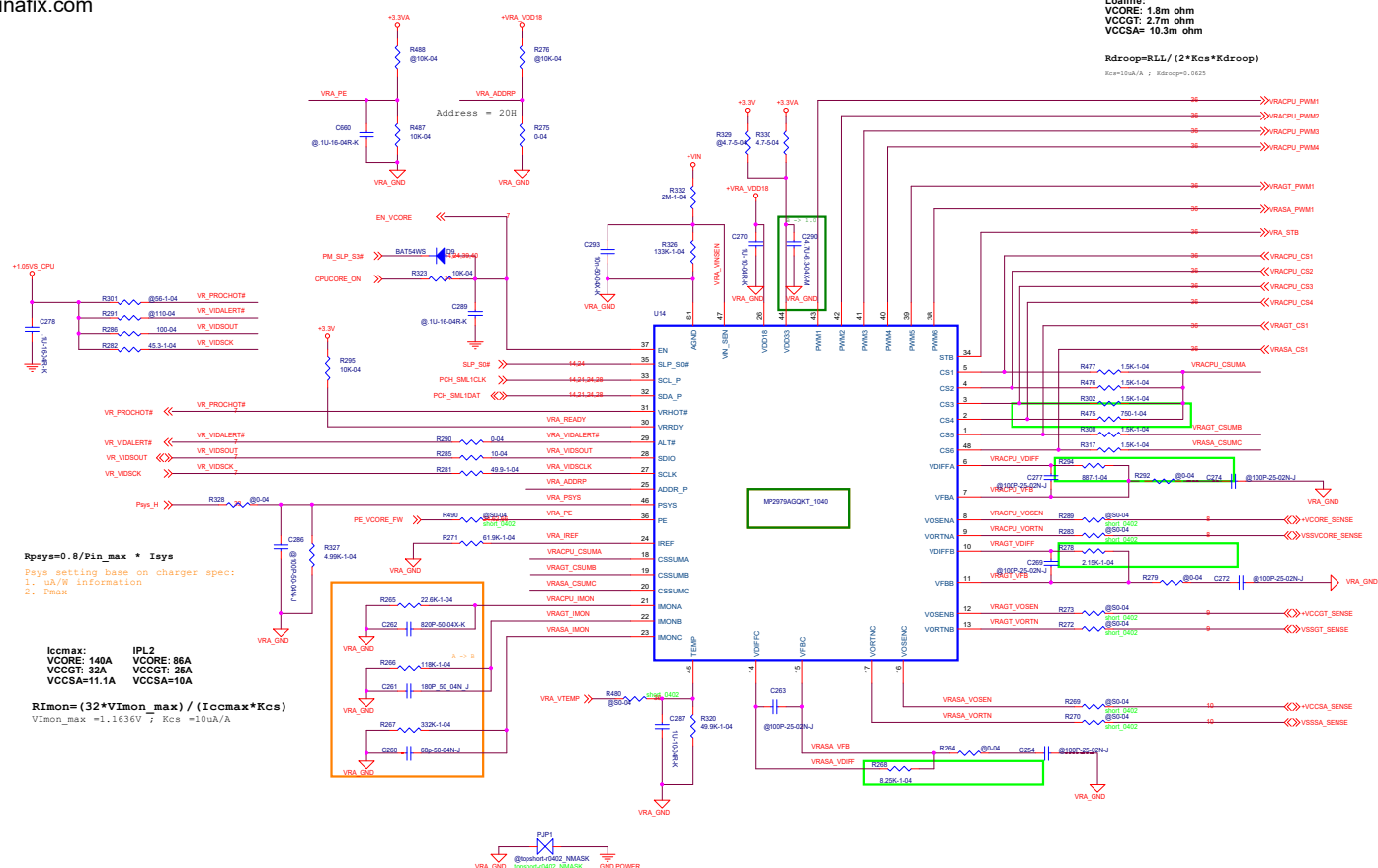
CPL



For RF solution



Loaline:
VCORE: 1.8m ohm
VCCGT: 2.7m ohm
VCCSA= 10.3m ohm

$$R_{\text{droop}} = R_{LL} / (2 * K_{cs} * K_{\text{droop}})$$
 $K_{ce}=10\mu A/A$; $K_{droop}=0.0625$ 

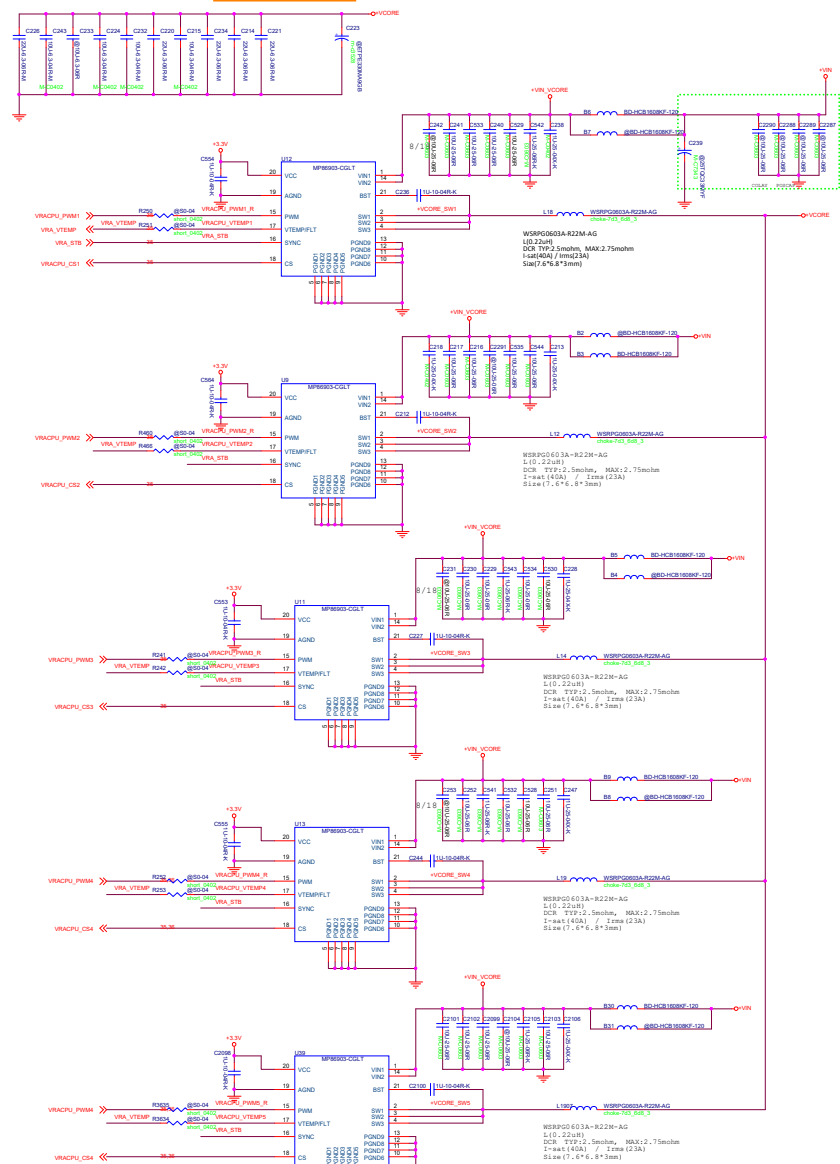
同方国际信息技术有限公司

Title				35 POWER VR CONTROLLER			
Size	Document	Number			Re		
Custom			GM7MGxx				
Date: Saturday, August 22, 2020				Sheet 35 of 70			

+VCORE

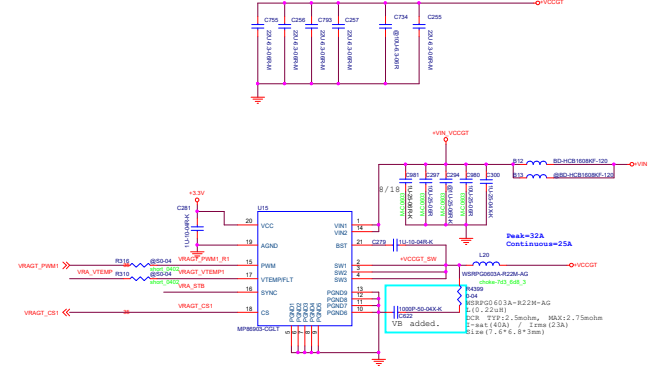
CML-H

VCORE: Iccmax=165A
VCORE: TDC=?A
PL2/PL4=135W/200W



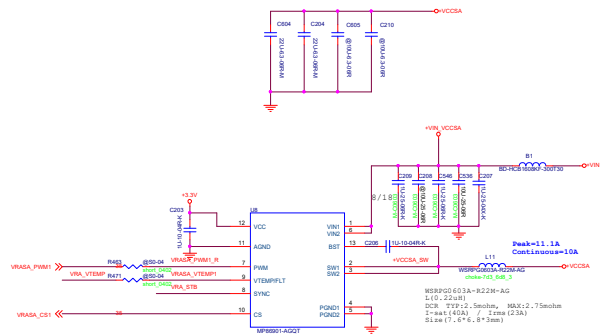
+VCCGT

```
VCCGT:  Iccmax=32A
VCCGT:  TDC=25A
```

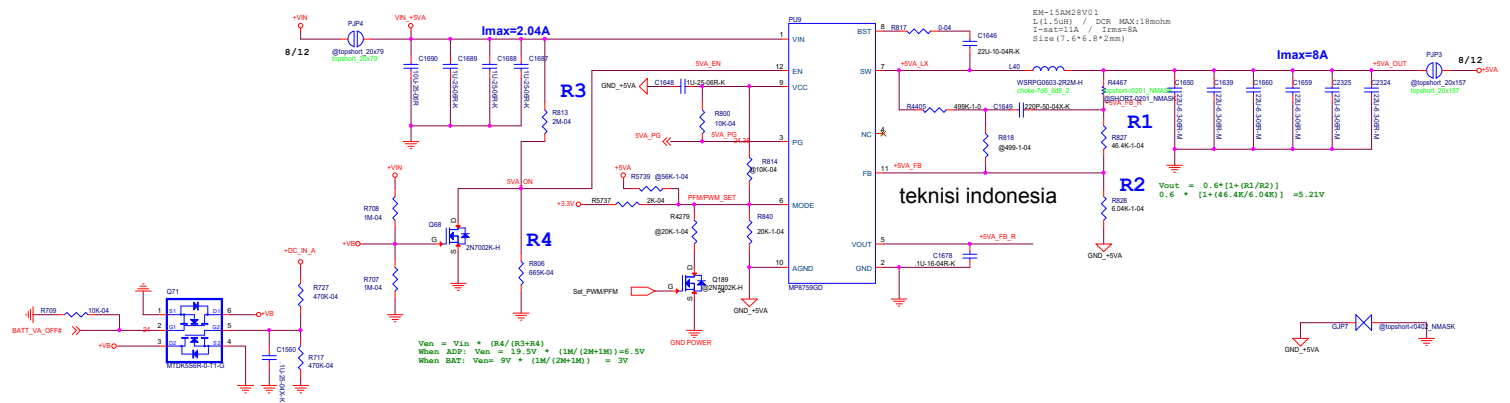


+VCCSA

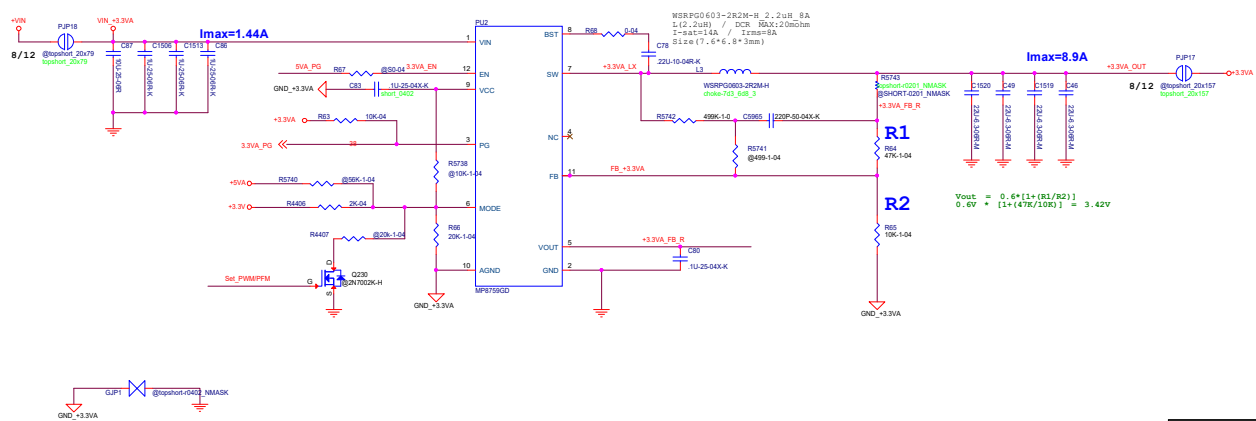
```
VCCSA: Iccmax=11.1A
VCCSA:TDC=10A
```



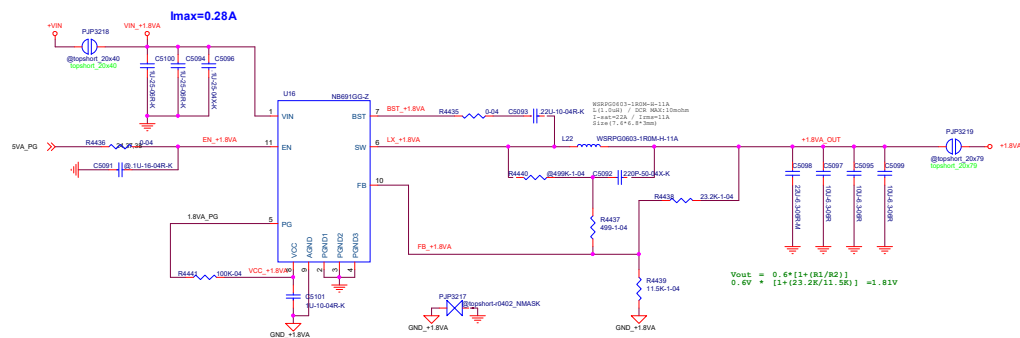
+5VA



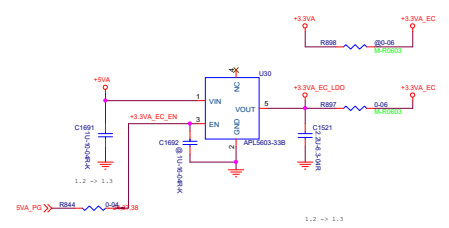
+3.3VA



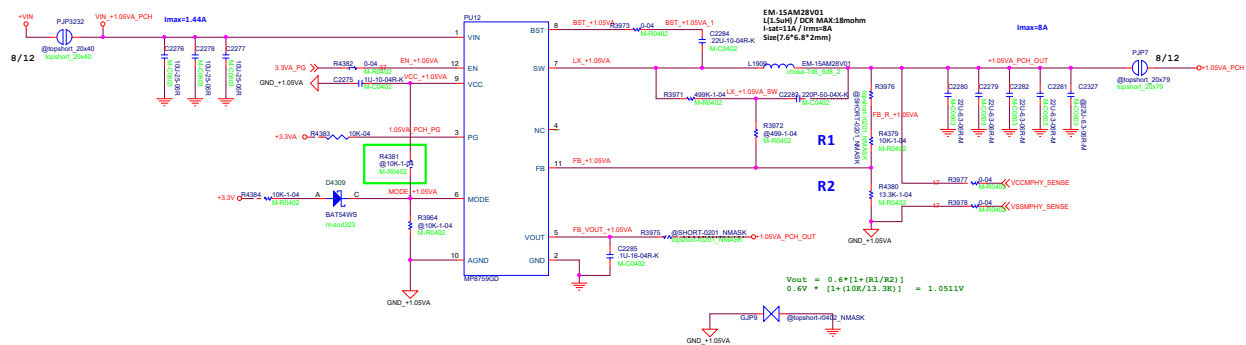
1.8VA Converter



+3.3VA_EC

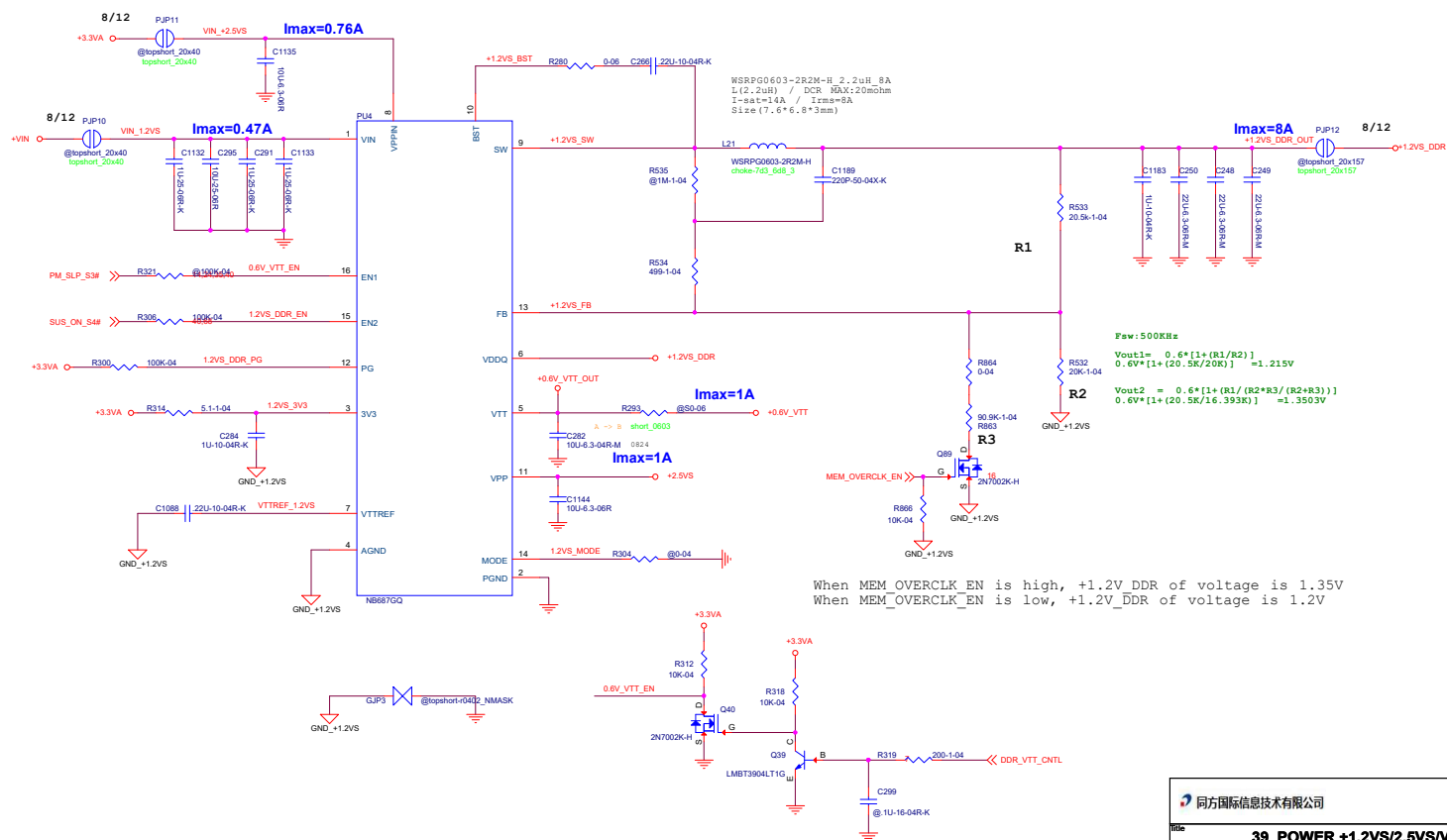


+1.05VA_PCH



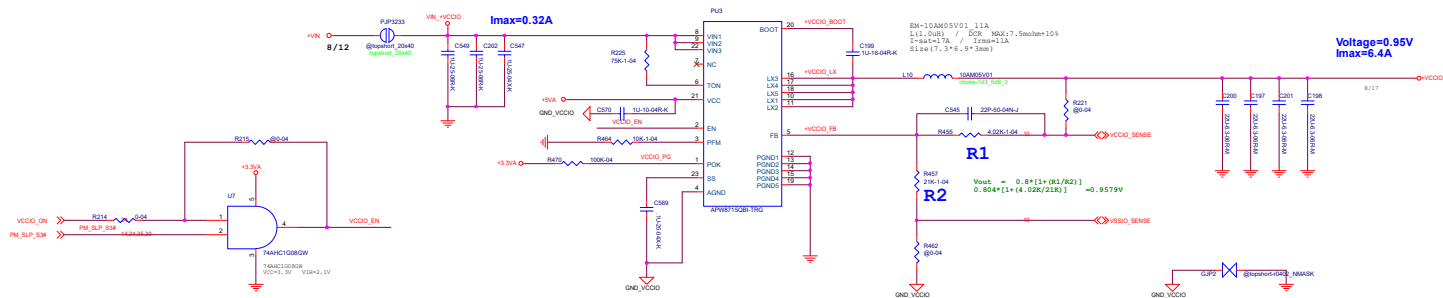
Vinafix.com

+1.2VS_DDR/+2.5VS/+0.6V_VTT

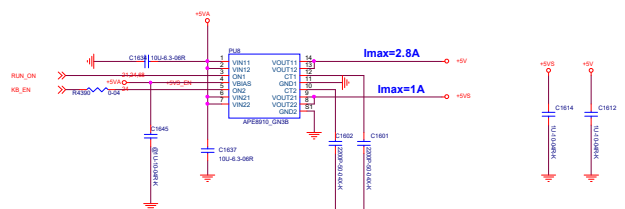


 同方国际信息技术有限公司			
Title 39_POWER +1.2VS/2.5VS/VT			
Size	Document	Number	Rev
Custom	GM7MGxx		A
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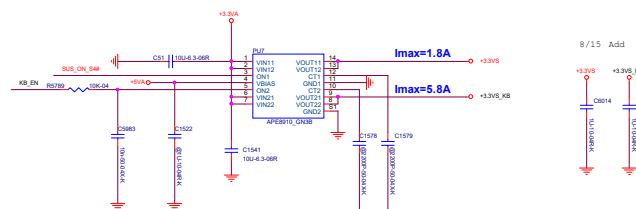
+VCCIO



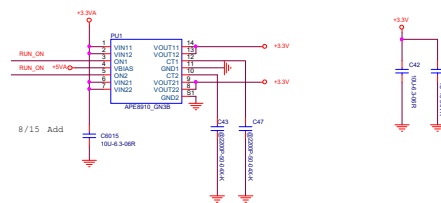
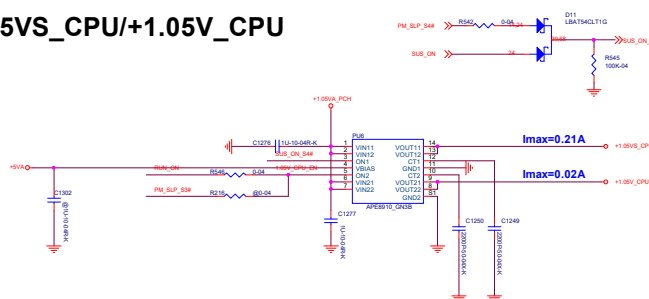
+5VS/+5V



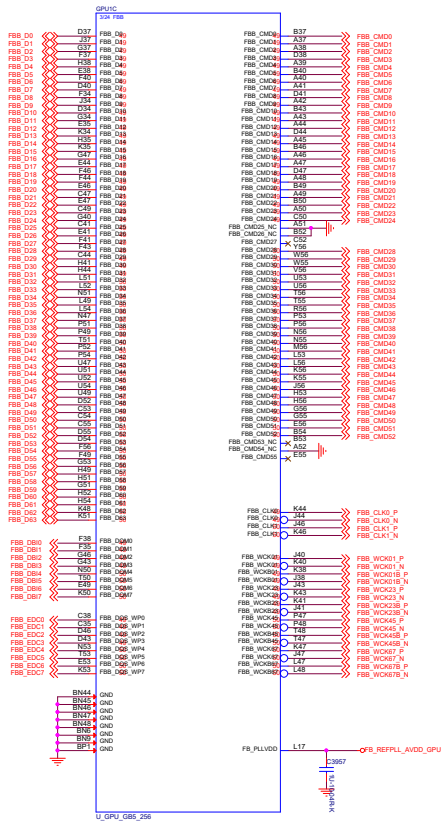
+3.3VS/+3.3V

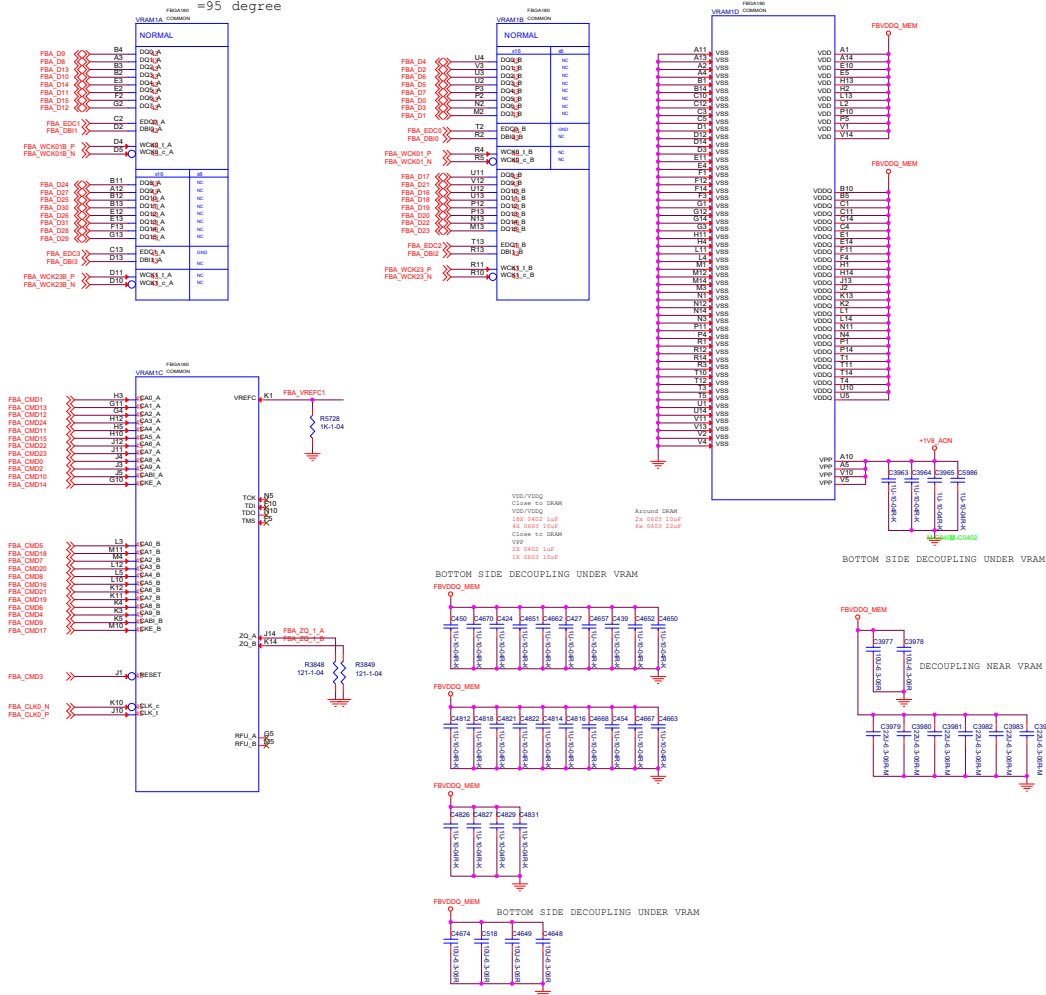


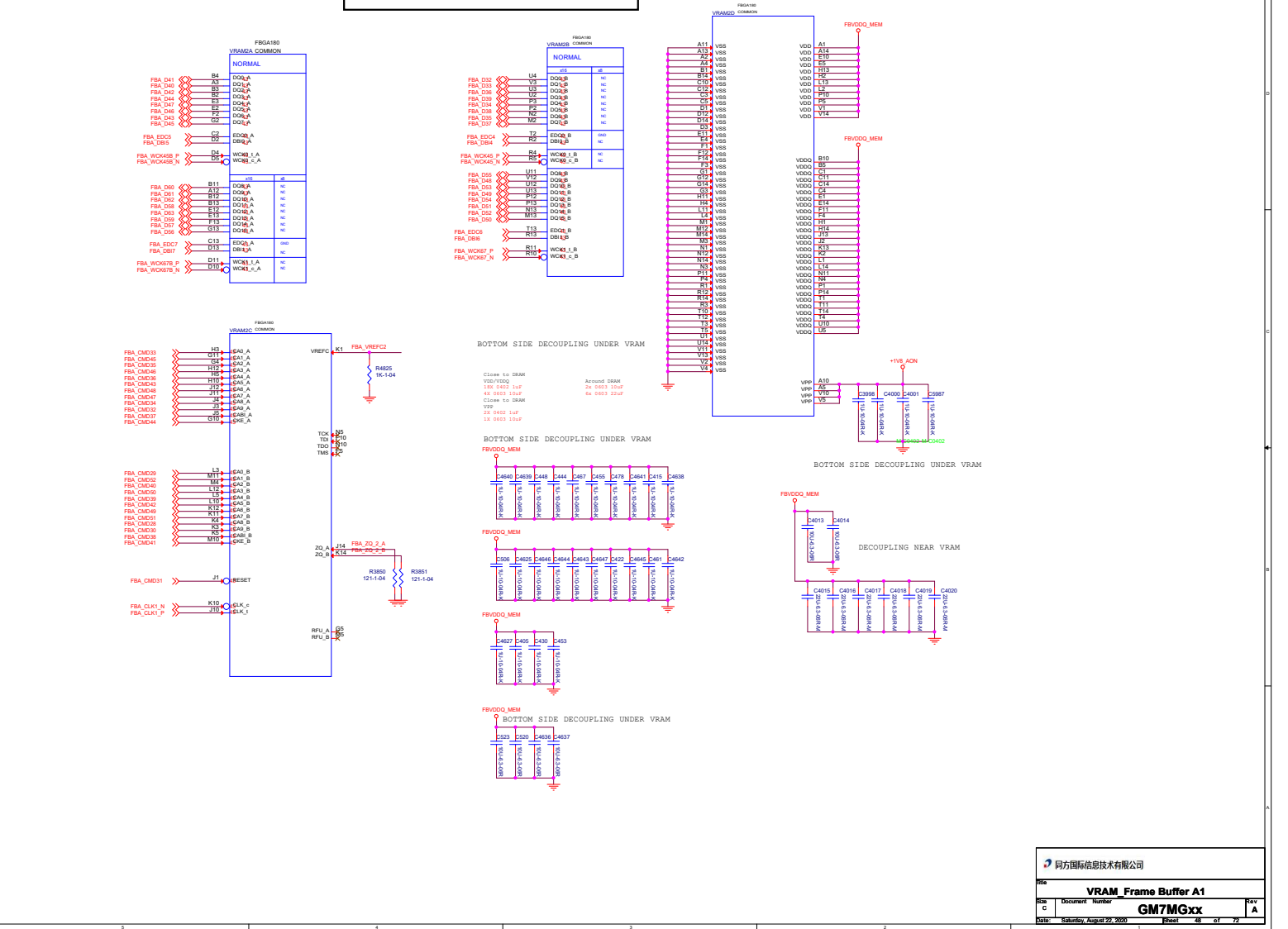
+1.05VS_CPU/+1.05V_CPU

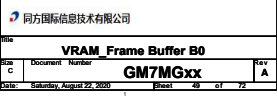


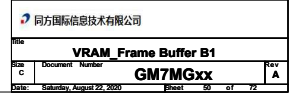
 同方国际信息技术有限公司			
Title			
GPU N18E GFX-PCIE			
Rev	Document Number	Rev	
C		GM7MGxx	
Date		Release	2025
Release		2025	2025



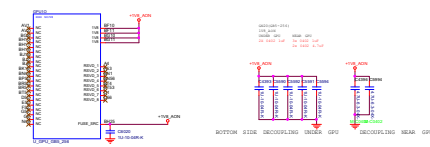
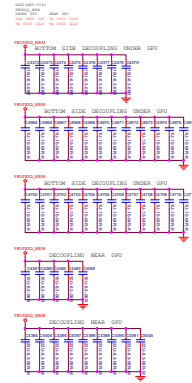
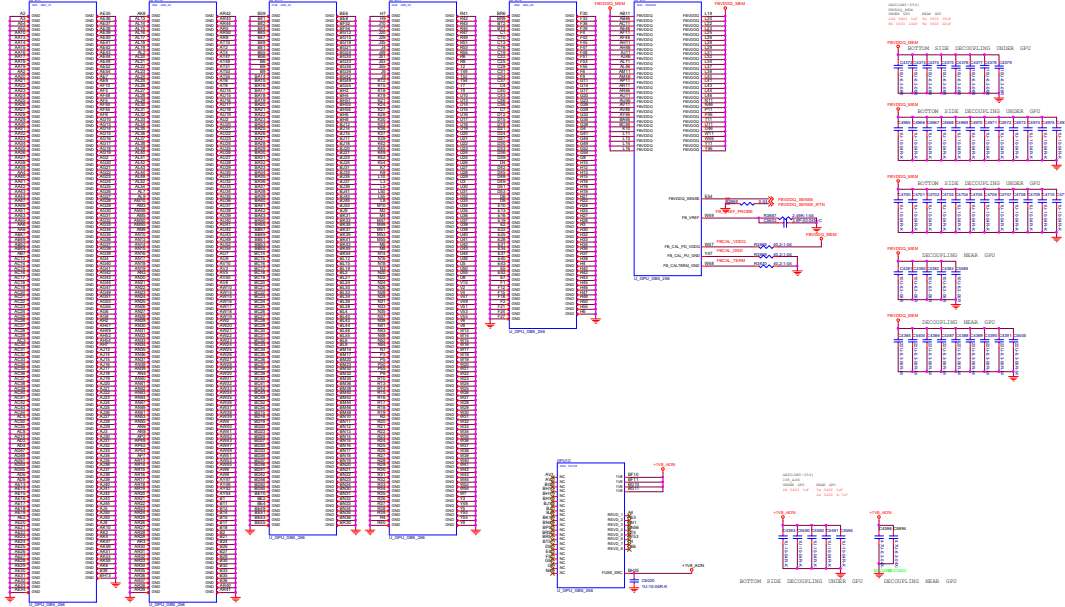






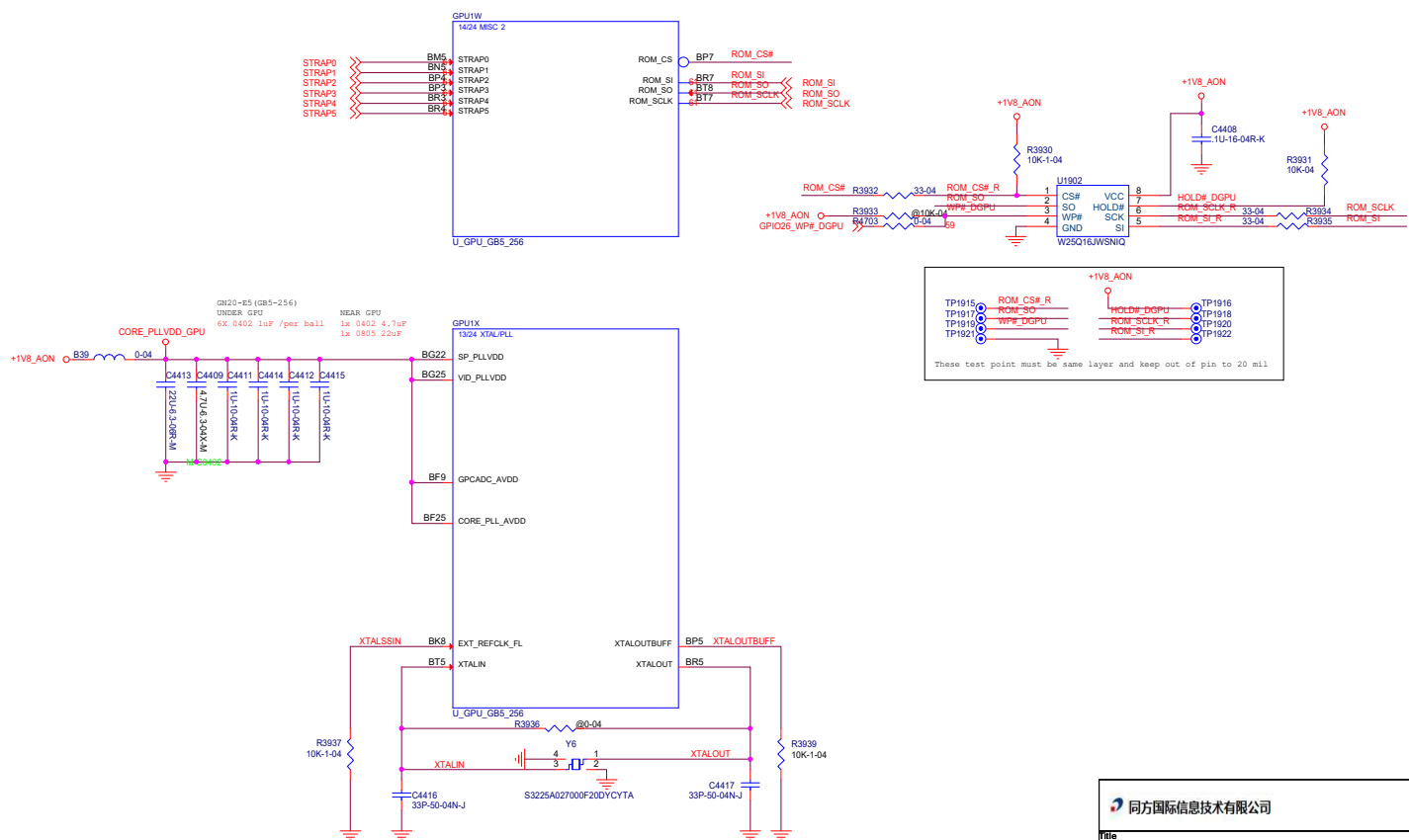







	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

 同方国际信息技术有限公司				
Title				
GPU N18E NVLINK				
Size A	Document Number			Rev A
	GM7MGxx			
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 同方国际信息技术有限公司			
File			
GPU N18E BIOS/XTAL			
Size B	Document Number	GM7MGxx	Rev A
Date:	Tuesday, August 25, 2020	Sheet 60 of 72	

Voltage(V)			
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

FS OVERT			
FUNCTION	ROM_SO	ROM_SI	ROM_SCLK
disable	L	L	L
enable	L	L	H

GN20-E5 GDDR6						
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H
8Gb	Hynix	H56C8H24AIR-S2C A-die	0X2	L	H	L

Strap5,4,3 LH			
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
0	0	0	1

Strap5,4,3 HLH			
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
0	1	0	1

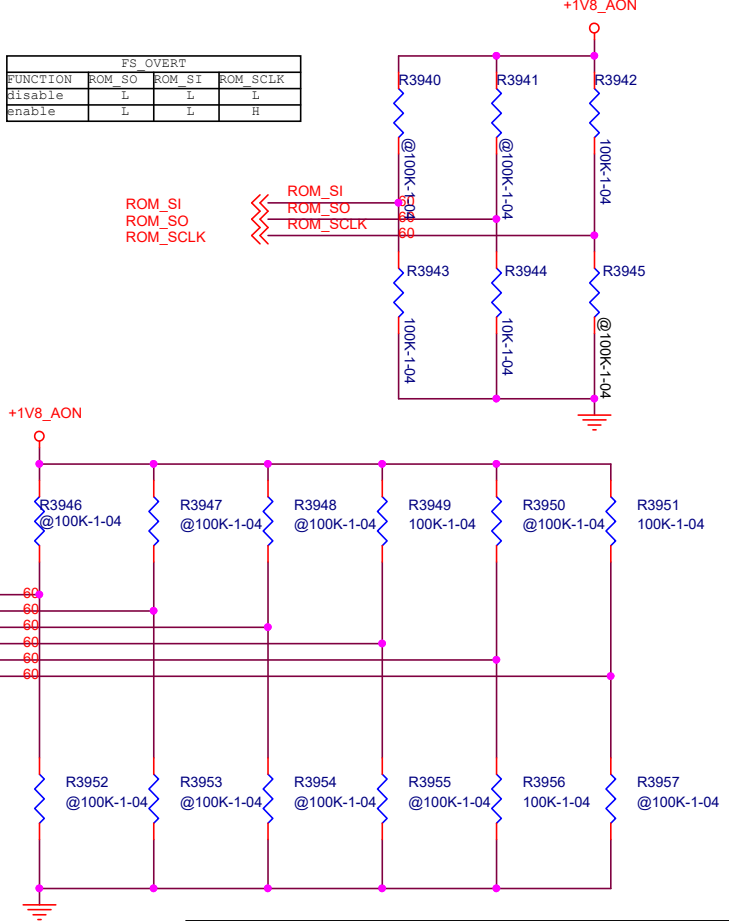
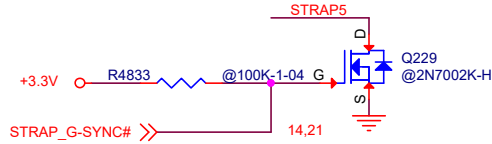
1:SMB_ALT_ADDR dual GPU alternate
0:SMB_ALT_ADDR single GPU

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG reduced signal amplitude
0:PCIE_CFG normal signal swing

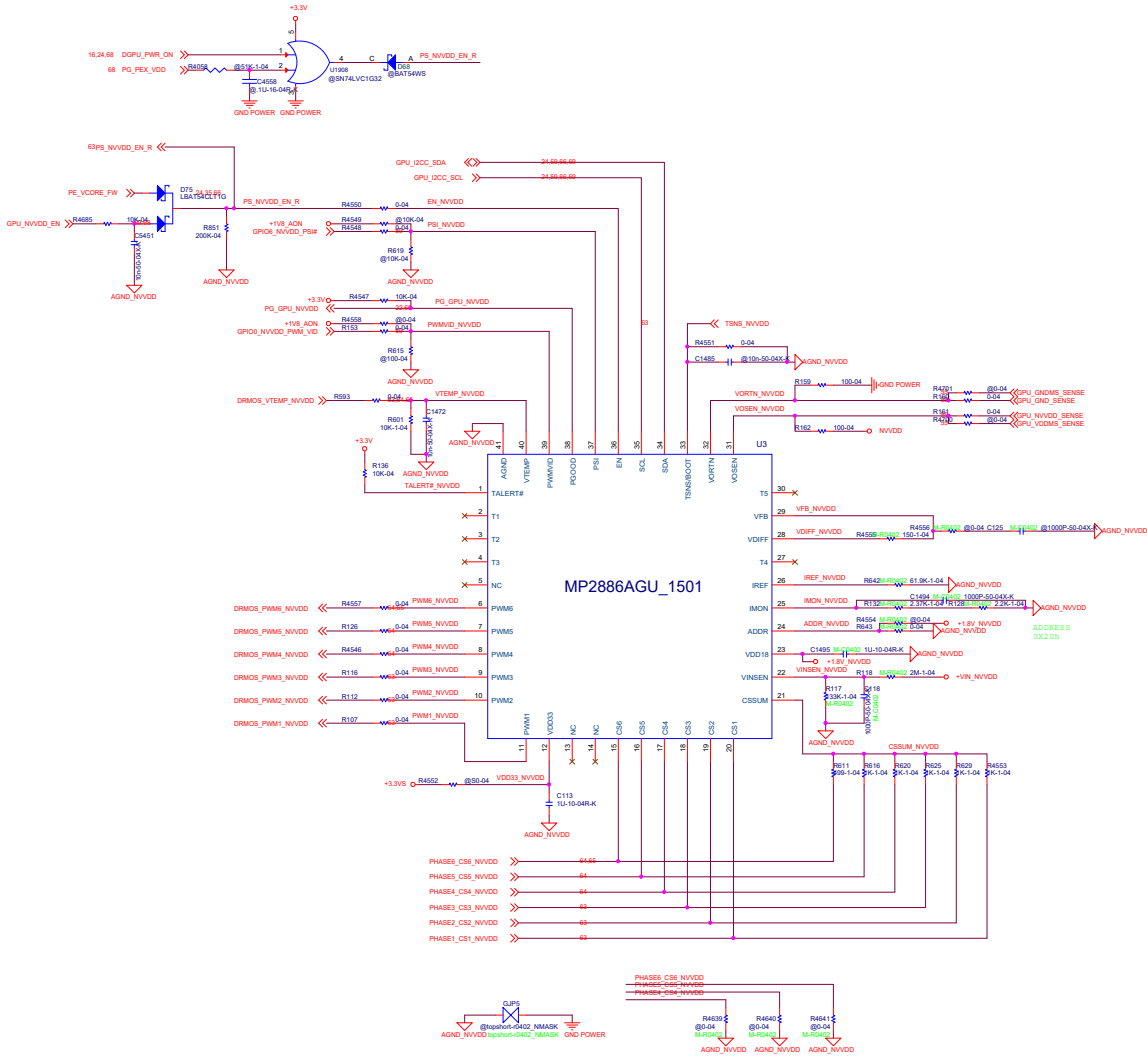
1:VGA_DEVICE class code 300
0:VGA_DEVICE class code 302

STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5

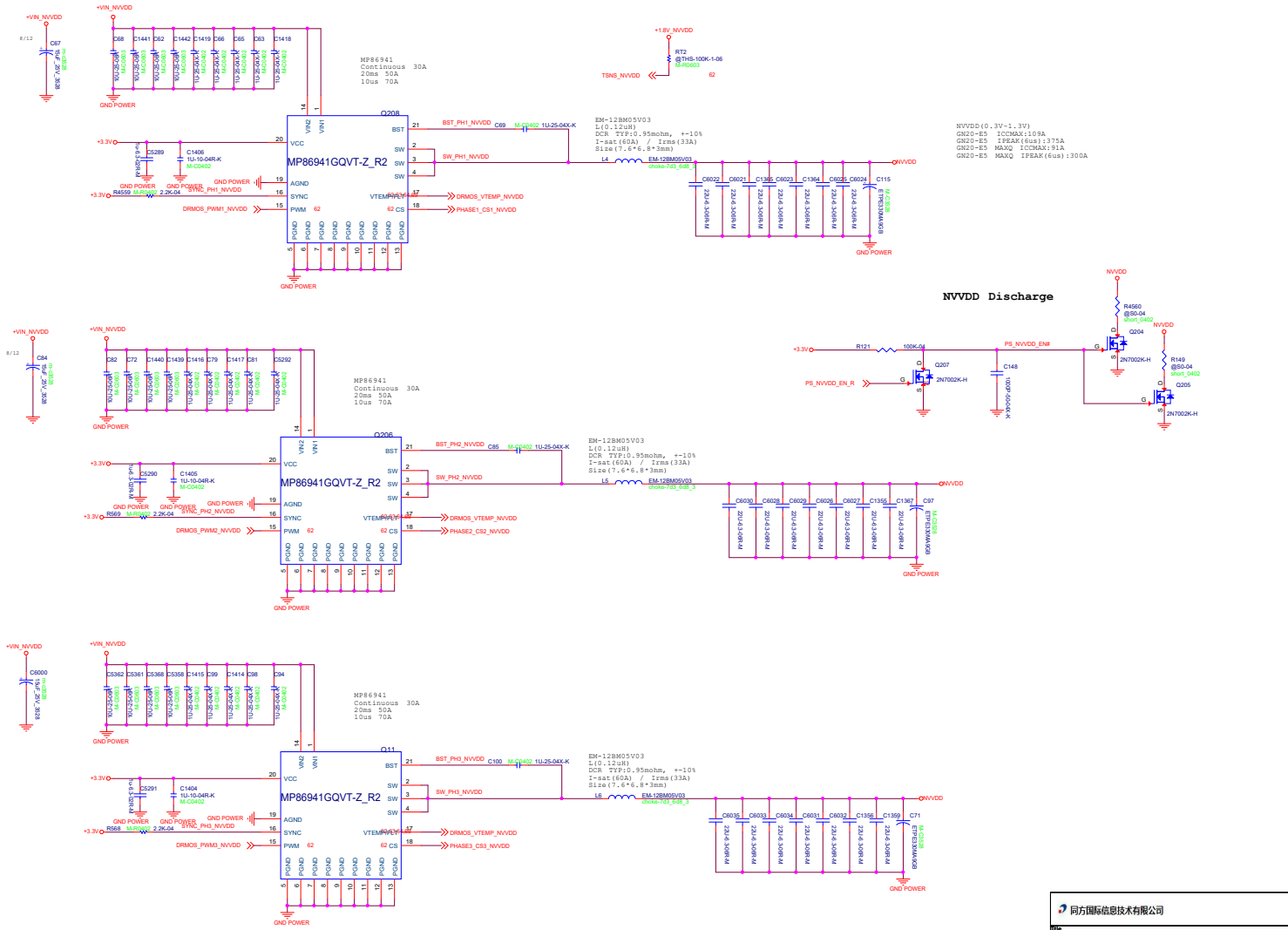


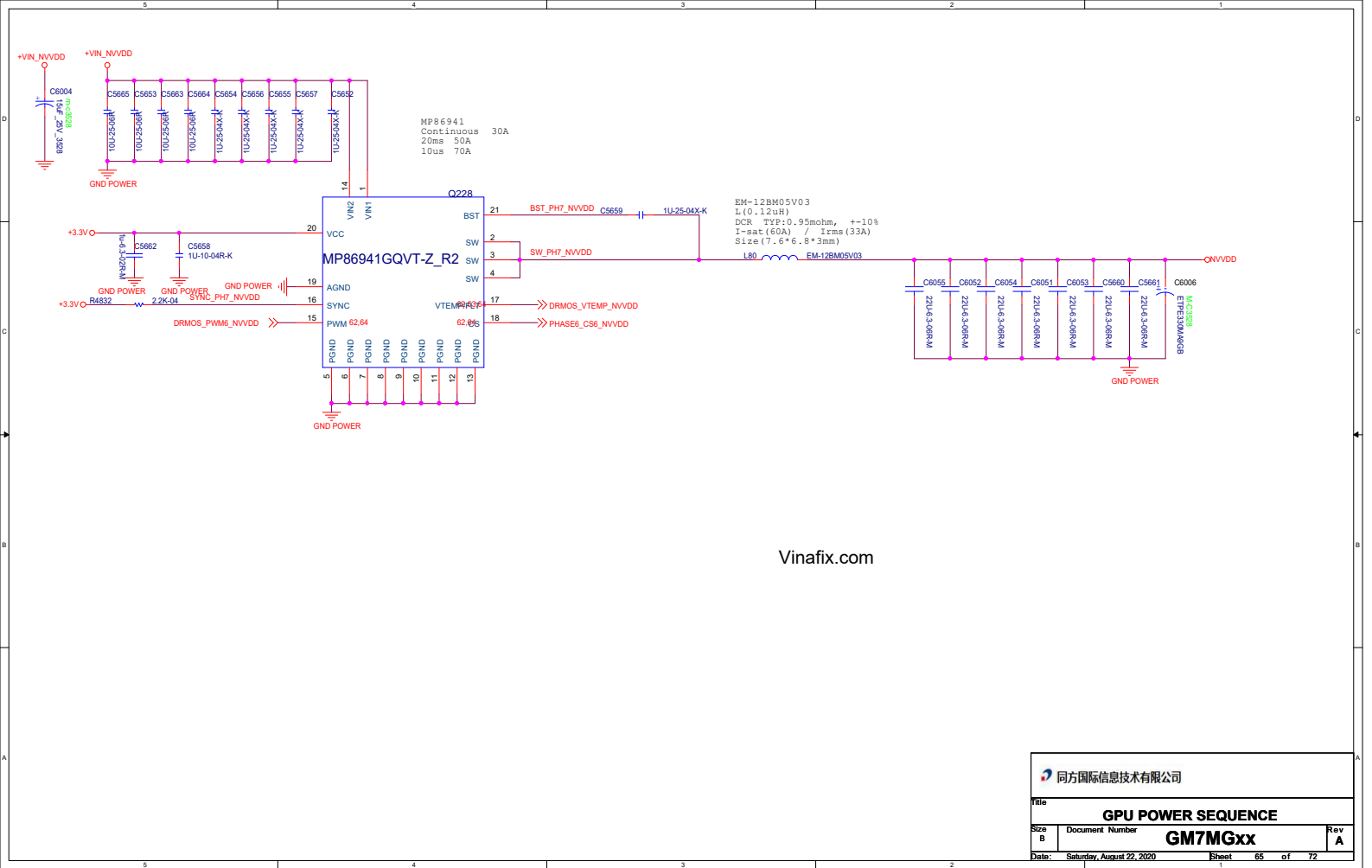
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Title		
GPU N18E STRAP		
Size A	Document Number	Rev A
	GM7MGxx	A
Date:	Saturday, August 22, 2020	Sheet 61 of 72

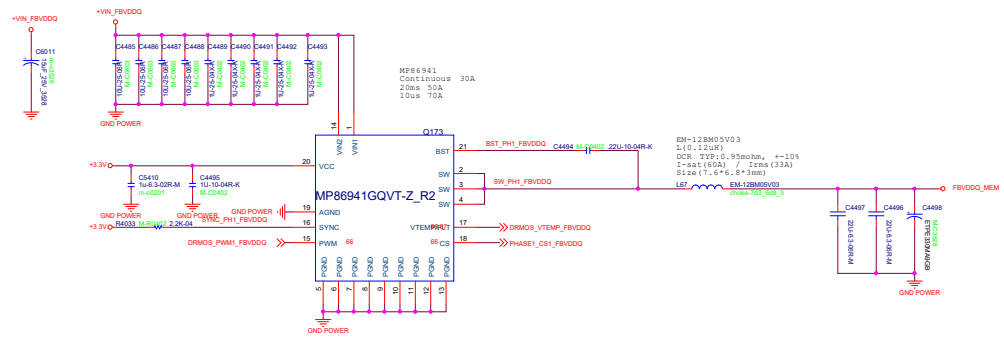


同方国际信息技术有限公司			
Title: POWER N18E NVDD CONTROLLER			
Rev: C	Document Number:	GM7MGxx	
Date: Monday, August 24, 2020	Sheet: 10	of	12

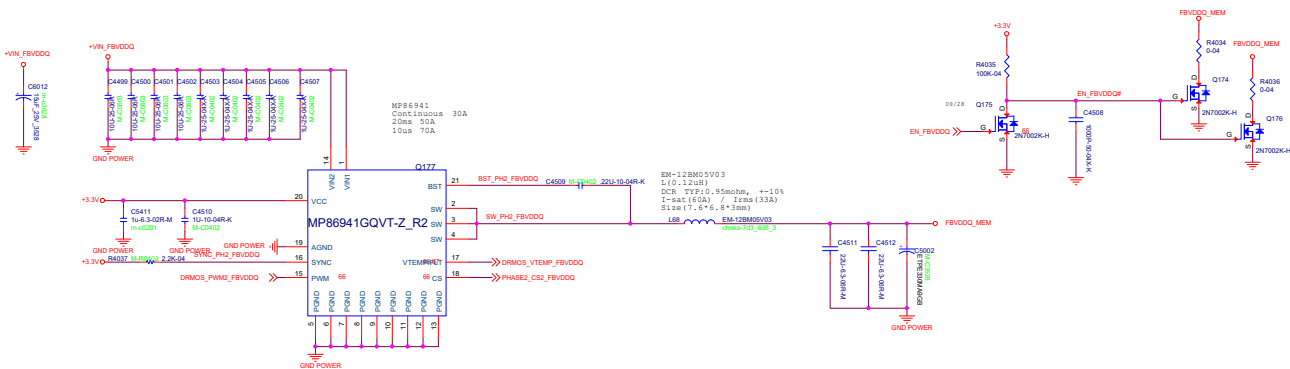






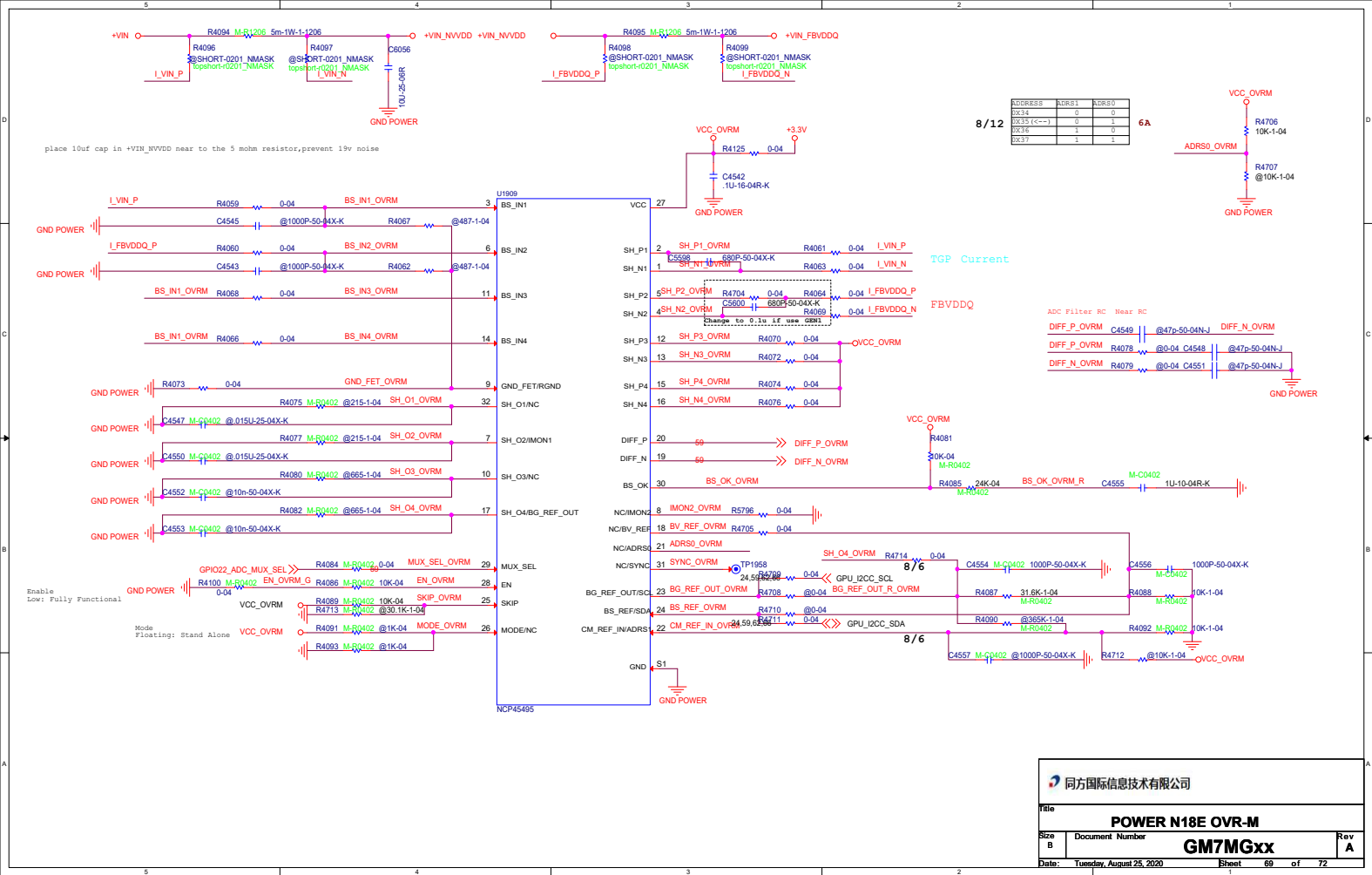


FBVDDQ_MEM Discharge



同方国际信息技术有限公司			
POWER N18E FBVDDQ 2PHASE			
Rev	Document	Number	Rev
C		GM7MGxx	A
Date		Validity	August 27, 2005
Sheet		01	12

+VIN VIN PEX VDD I_{max}=0.28A



No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	B1-1 Add capacitor for D05 AUXPAN solved non-D05 L5 panel no display	C8037,C8038	Schematic&BOM&Layout	27
2	B1-2, Change R733 value for D8 thermostat	R733(10K to 47K)	Schematic&BOM	36
3	B1-3, Change R3661 value	R3661(47K to 10K)	Schematic&BOM	36
4	B1-4, Changed power plane V16_AON to +3.3V_LCD for pull up	R4364,R4365	Layout	64
5	B1-5, Changed C443 value for ME interference	C433(bx EEEH6 IE130L)	BOM	46
6	B1-6, Changed U1908 PCB footprint	U1908	Schematic&Layout	72

1. Add jumper for power
2. C1333 stuff
3. R102 R104 should support R102: pending
4. Modify C12 address
5. R5744 (Stub to 100K)
6. Add C1611&C1612
7. Del 100K_W1701 (N1&N2)
8. U1908&U1909 exchanged Pin
9. Changed R11&R12&R13 PCB footprint
10. Del R2021&R2022
11. Add media_upgrade connector
12. Modify CPU power V16 input impedance stuff/default
13. Add new input output manual 4

14. Del 100K_W1701
15. Add C1611&C1612 to 100K
16. Change V16_W1701 to 100K
17. Change C1611&C1612 to 100K
18. Change C1611&C1612 value 4.7K to 2.2 K page 59
19. pull down C1611&C1612 V value to 100K page 59
20. Change C1611&C1612 value to 100K page 59
21. remove pull up C1611 page 61
22. delete C1611&C1612,add C1611
23. Add media_upgrade C1611&C1612 page 61&62
24. pull up 10 K&10K,commented page 59
25. delete C1611&C1612,commented C1611 page 59
26. delete stuff C1611 page 59
27. Add pin_V16_W1701 and C1611&C1612 page 61
28. Add C1611&C1612 value 100K and C1611 page 61
29. commented C1611&C1612 page 61
30. delete C1611&C1612 page 61, delete C1611&C1612 page 61, delete C1611&C1612 page 61
31. Add C1611&C1612 to 100K for 47 ohm page 61
32. Add C1611&C1612 to 100K for 47 ohm page 61